Controlling Critical Innovation Inputs: Semiconductors in U.S.–China Technology Competition

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Abstract

We document novel evidence that semiconductors are a critical innovation input whose price declines and technological advancements drive downstream R&D, making semiconductor sanction policies amid U.S.–China technology competition highly consequential for growth and welfare. To evaluate counterfactual regimes, we develop and estimate a two-country endogenous growth model in which semiconductor firms innovate strategically along a quality ladder and downstream firms use semiconductors in innovation. Export controls reallocate chips from China to the U.S., raising U.S. downstream innovation while reducing Chinese counterpart. Restrictions on semiconductor technology diffusion raise the returns to U.S. technological leadership and stimulate U.S. innovation. Although the market scale loss ultimately dampens long-run growth in both countries, the trade and technology restrictions generate net welfare gains for the U.S. They also amplify U.S. gains while nearly eliminating China's gains from an AI boom. A larger pre-sanctions U.S. technological lead would yield a smaller innovation response, providing an economic rationale for imposing controls when the U.S.–China technology gap is narrow.

Keywords: Industrial policy, economic growth, U.S.-China technology competition, innovation.

JEL classification: F40, O10, O30, O40, O50.

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1 Introduction

Semiconductors are a critical input into modern innovation. As innovation becomes increasingly data-intensive, computational advances raise R&D productivity by enabling precise sensing, large scale data collection and analysis, and development and training of more capable machine-learning and AI models. Semiconductors therefore fit the classic conception of a general-purpose technology (GPT, Helpman 1998), creating "innovational complementarities" that raise the returns to downstream invention and stimulate R&D across user industries.

Semiconductors are also at the core of the ongoing U.S.–China technology competition. The U.S. semiconductor sanctions against China restricted China's access to (1) advanced chips and (2) the technology needed to produce them. Their stated objective is national security: U.S. policymakers emphasize preventing advanced semiconductors and related technologies from supporting China's military modernization and military–civil fusion strategy (U.S. Department of Commerce, 2023). Although this national-security rationale is explicit and well understood, the broader economic consequences of these controls—for innovation, growth, and welfare in both countries—remain much less clear.

Semiconductor controls affect economic growth through several, potentially offsetting, channels. Limiting Chinese access to high-quality chips may constrain China's downstream R&D. At the same time, reallocating chip supplies away from China could improve access for U.S. downstream firms, supporting U.S. innovation particularly amid surging AI demand. The controls also affect innovation within the semiconductor sector. A less competitive domestic market gives Chinese chipmakers stronger incentives to innovate, yet restricted access to U.S. technology hampers their catch-up and innovation. By reducing the likelihood of Chinese catch-up, these restrictions could raise short-run returns to U.S. semiconductor leadership and innovation. Over time, however, reduced access to the Chinese market could limit scale and slow semiconductor growth. Any resulting change in semiconductor innovation can, in turn, propagate to downstream innovation and growth.

In this paper, we first document novel empirical evidence that semiconductors operate as a GPT: declines in semiconductor prices and advances in semiconductor technology stimulate downstream innovation. To evaluate policy trade-offs, we provide the first quantitative assessment of counterfactual semiconductor control regimes, rather than evaluating the realized ex-post effects of the 2022 U.S. controls. We develop a two-country endogenous growth model in which countries innovate in quality-differentiated semiconductor and downstream sectors, trade in both sectors, and technology spills over from the leader to the follower. Downstream innovation depends on semiconductors, allowing the model to capture the multiple channels through which semiconductor controls affect innovation and growth. We calibrate the model to cross-country differences in U.S. and

Chinese patenting across semiconductor technology classes, as well as to the estimated elasticities of downstream innovation with respect to semiconductor price and innovation shocks.

We find that restrictions on semiconductor exports to China stimulate U.S. downstream innovation while harming Chinese downstream innovation. Restricting technology spillovers raises the returns to technological leadership, which increases U.S. semiconductor innovation. Although market scale loss ultimately reduces innovation and growth in both countries in the very long run, the controls generate net welfare gains for the United States. These gains are larger during an AI boom, when reallocating chips toward U.S. downstream innovation is especially valuable. They are also larger when U.S. and Chinese semiconductor technologies are neck-and-neck (as in the early 2020s), as a narrow technology gap amplifies the escape-competition returns to restricting knowledge spillovers.

Our first step is to document the effects of cheaper semiconductors on downstream innovation using local projections. We use changes in semiconductor tariffs as shocks to their prices, combining cross-country data on semiconductor imports, input–output linkages, and patent filings at a granular sectoral level. Because domestic economic conditions may confound semiconductor tariff changes, we instrument semiconductor tariffs with changes in Most-Favored-Nation (MFN) semiconductor tariffs applied to non-major import source countries. Driven largely by the global phase-in of the WTO Information Technology Agreement, these MFN tariff changes, in particular if they are applied to non-major trade partners, are unlikely to be driven by conditions in the importing country. We find that lower semiconductor tariffs increase downstream innovation, as measured by patent filings and citations, but have weaker effects on downstream production or employment that dissipate more quickly. These effects stand in contrast to those of ordinary production inputs, whose tariff changes have much weaker effects on downstream innovation.

Next, we examine how semiconductor innovation affects innovation across sectors and countries. Using detailed patent data from the Orbis Intellectual Property database, we construct a measure of each country–sector's exposure to domestic and foreign semiconductor innovation based on historical citation shares at the country–IPC-code level. The data also allow us to distinguish between high-end and low-end semiconductor technologies: we classify a technology as high-end if, in recent years, U.S. patenting in the corresponding IPC code exceeds Chinese patenting. Using local projections, we find that semiconductor innovation stimulates innovation in other sectors, and high-end semiconductor innovation increases downstream innovation more. We establish causality by instrumenting U.S. semiconductor innovation through U.S. domestic R&D shocks. Finally, U.S. semiconductor innovation leads to subsequent semiconductor innovation in China, highlighting cross-border technology diffusion and that restricting these technology flows could slow China's semiconductor catch-up.

To evaluate the impact of controlling semiconductor trade and technology on growth and welfare in the U.S. and China, we develop a two-country endogenous growth model with rich general equilibrium dynamics. Each economy features a semiconductor sector and a downstream sector. In the semiconductor sector, firms engage in step-by-step innovation along a quality ladder and compete oligopolistically within their quality tier. Innovation incentives are governed by endogenous markups, market shares, and bilateral technology gaps, generating a realistic semiconductor quality distribution. In the downstream sector, firms use semiconductors as essential innovation inputs; semiconductor prices and technological progress shape downstream R&D intensity and aggregate growth. Downstream output re-enters as production and R&D inputs, capturing input–output linkages. Finally, the model incorporates international trade in both semiconductor and downstream goods, as well as cross-country knowledge diffusion.

We calibrate the model's key parameters using the simulated method of moments (SMM). For the semiconductor sector, the core parameters govern each country's innovation efficiency and the rate of technology spillovers from leader to follower. We estimate these parameters by matching the model-implied quality distribution to the empirical distribution of patenting differences across IPC codes between the U.S. and China, while also targeting cross-border semiconductor innovation spillovers. For the downstream sector, we calibrate the elasticity of R&D with respect to semiconductors by targeting our empirical estimates of how semiconductor price shocks and technological advances drive downstream innovation.

Consistent with the design of actual policies, we model semiconductor sanctions as two different components: export controls and restrictions on technology diffusion. Export controls limit trade in advanced semiconductors, which we define as product varieties in which the U.S. leads China technologically. We map these varieties empirically to IPC codes for which U.S. patenting has exceeded Chinese patenting in recent years. Restrictions on technology diffusion, in turn, lower the exogenous probability that a technologically lagging firm catches up to its foreign rival's frontier.

Semiconductor control policies boost U.S. innovation in both the semiconductor and downstream sectors in the short and medium run, producing net welfare gains for the U.S. Innovation gains in the semiconductor sector are driven primarily by restrictions on knowledge diffusion, which raise the returns to technological leadership. Simultaneously, reduced chip sales to China reallocate supply toward the U.S., driving downstream innovation. Greater downstream innovation further benefits semiconductor innovation by providing larger demand for semiconductors and cheaper inputs for semiconductor innovation. These two mechanisms reinforce each other and widen U.S. technological lead over China in both sectors. Losing access to the Chinese market reduces the scale returns to U.S. semiconductor innovation only in the very long run, ultimately depressing semiconductor and downstream R&D. Nevertheless, the short-run innovation and growth benefits

dominate, yielding an overall U.S. welfare increase of 1.1%.

Semiconductor control policies reduce Chinese welfare by 0.8%. Upstream, Chinese semiconductor innovation experiences two opposing forces: restricted technology spillovers depress innovation, whereas export controls generate import-substitution incentives for Chinese chip R&D. Quantitatively, we find that the latter dominates, yielding a net increase in Chinese semiconductor growth. Downstream, however, the policy impact is unambiguously negative. Restricted access to advanced semiconductors depresses downstream R&D and growth, which drives China's net welfare loss. An increase in China's semiconductor innovation efficiency (reflecting subsidies towards chip R&D) decreases China's welfare loss while simultaneously increasing welfare gains for the U.S., because U.S. firms gain access to higher-quality Chinese semiconductors.

The macroeconomic effects of semiconductor controls depend critically on the downstream innovation environment governing chip demand. In an AI-boom scenario—where downstream innovation efficiency for a given level of semiconductor inputs increases by 5%—absent any controls, welfare rises by around 1.7% in both the U.S. and China. However, because export controls induce relative chip abundance in the U.S. and shortages in China, while technology controls accelerate U.S. semiconductor innovation and depress Chinese innovation, the combined policies amplify U.S. innovation and growth across both sectors while widening bilateral technology gaps. Ultimately, the controls increase the U.S. welfare gain from the AI boom to 2.0%, while reducing the Chinese welfare gain from the AI boom to near zero.

The effects of semiconductor controls also depend on the technology gap between the U.S. and China when policies are imposed. When semiconductor sanctions were introduced in 2022, which serves as the initial steady state in our model, the semiconductor technology gap between the U.S. and China had narrowed significantly. In this near neck-and-neck environment, restricting knowledge diffusion increases the leader's payoff from innovation, substantially raising U.S. semiconductor firms' incentives to innovate to escape competition from China. By contrast, had controls been imposed in 2010, when the U.S. held a substantial technological lead and the return to further innovation was lower, the policy would have generated a much smaller growth boost and a overall welfare loss for the U.S. This state-dependent return to leadership provides an economic rationale for why the U.S. enacted semiconductor restrictions in recent years rather than a decade earlier.

Related Literature. We contribute a multi-country, multi-sector step-by-step innovation model to the trade and innovation literature (e.g., Eaton and Kortum 1999, Atkeson and Burstein 2010, Bustos 2011, Sampson 2023, Bai et al. 2023, Santacreu 2025, Chen et al. 2023, Liu and Ma 2023). While prior studies typically assume a representative firm within each country–sector, our framework allows U.S. and Chinese semiconductor firms to strategically innovate along a quality

ladder subject to cross-border spillovers. We extend standard step-by-step growth frameworks (see, e.g., Aghion et al. 2001, Aghion et al. 2005, Akcigit et al. 2018, Sui 2023) by incorporating downstream innovation that uses semiconductors as essential inputs, capturing the aggregate growth impacts of upstream strategic rivalry in an open-economy environment.

Second, we provide new empirical evidence on the links between semiconductor and downstream innovation. Prior economic studies on semiconductors focus primarily within the industry, examining pricing, market structure, and market shares (Irwin and Klenow 1994; Aizcorbe and Kortum 2005; Miao 2023). In contrast, we demonstrate that semiconductors function as a GPT, whose price reductions and technological advances stimulate downstream innovation. Hence, semiconductor control policies, which alter semiconductor prices and innovation through trade and knowledge diffusion barriers, affect growth across the global economy.

Third, we contribute to the literature on geopolitics and sanctions (see, e.g., Becko and O'Connor (2024); Clayton et al. (2026); de Souza et al. (2024); Deseatnicov and Fukao (2024); Egorov et al. (2025); Flynn et al. (2025); Han et al. (2024); Kleinman et al. (2020, 2024); Li et al. (2024); Liu et al. (2024, 2025); Thoenig (2024)). We contribute to this literature by introducing a quantitative framework to evaluate trade and technology-diffusion restrictions on critical innovation inputs, which are the policy tools at the very center of the U.S.–China technology rivalry. We show that such controls can generate domestic innovation and welfare gains, extending beyond the traditional national security objectives emphasized in previous literature. Unlike earlier quantitative studies on sanctions that focus on general goods, relative prices, and production input–output linkages, our framework highlights traded inputs that are essential for downstream R&D and whose technological progress is driven by strategic competition and knowledge diffusion.

Roadmap. The rest of the paper proceeds as follows. Section 2 presents data construction and empirical findings. Section 3 develops the model and clarifies mechanisms. Section 4 describes parameterization and counterfactual transition-path results. Section 5 concludes.

2 Semiconductor as Critical Innovation Input

We present empirical evidence that establishes semiconductors as a critical upstream input for innovation in downstream sectors. We exploit two sources of variation that point to distinct—though inherently difficult to disentangle—channels. First, variation in importing countries' semiconductor tariffs affects downstream firms' costs of, and access to, semiconductors, capturing the effects of semiconductor *product flows*. Second, innovation in semiconductors, measured by patenting

activity, affects the quality of semiconductor technology inputs available to downstream sectors, pointing to *technological spillovers*.

We present suggestive evidence on semiconductor technology diffusion across the border in Appendix B.7, by looking at how semiconductor innovation in advanced economies associate with semiconductor innovation in developing economies, which also serves as an important assumption validation for our model.

Semiconductor concordance. We use public aggregate, firm-level, and patent-level datasets. Our empirical analysis of tariff variation is conducted at the industry level, whereas tariffs are measured at the HS product level. Semiconductor products are defined by native HS headings, mainly 8541, which covers semiconductor devices, and 8542, which covers integrated circuits. In robustness checks, we also include semiconductor-manufacturing equipment under HS heading 8486.

We construct each downstream sector's semiconductor expenditure share using BEA input-output tables. The BEA industry classification is based on NAICS, with NAICS 3344 as the main semiconductor code.[1] In analyses that require firm-level information, we map ORBIS industry codes to BEA sectors using the NAICS/NACE concordance. Specifically, we first convert firm-level ORBIS sectors to NAICS industries and then aggregate them to the BEA input-output sectors used to construct the production and exposure measures. Appendix Tables B.1, B.2, and B.3 list the identified semiconductor codes across these sectoral and product classification systems.

To identify semiconductor patents using the WIPO IPC Classification Scheme (2025-01-01 edition), we examine IPC class descriptions and identify those matching any of more than 30 semiconductor-related keywords.[2] Although patents may not capture all of firms' innovation activities, they provide the best available and most reliable measure of innovation. The data cover patents filed at approximately 40 patent offices worldwide. We focus on the period beginning in 1990.

A patent family and its normalized forward citations. A single invention is typically filed at multiple patent offices (e.g. the USPTO, EPO, JPO, and SIPO). In our patent-level dataset, ORBIS IP, a filing at each office appears as a separate row, with all filings sharing a common family ID. Naively summing patent counts across offices would therefore double-count (or triple-count, etc.) the same invention. We thus use the patent family as the unit of analysis.

When we use a patent's total forward citations to measure its quality or influence, we must also

[1] When a finer concordance is available, we also include semiconductor and related device manufacturing industries (e.g., NAICS 334413).

[2] See Appendix Table B.4 for the list of keywords. Major identified semiconductor IPC classes include H01L, H10B, H10H, H10K, H10N, and G11C.

make citation counts comparable across offices. A forward-citation count at SIPO may not be on the same scale as one at the USPTO or EPO. Absolute citation counts can differ across patent offices even for technologically equivalent patents because examination practices vary across offices and the pool of *citing* patents is largely local to each office. Pooling raw citation counts across offices would therefore over-weight large offices and jurisdictions with large citation pools.

Thus, for each patent j filed at office p in year t, we define office-year-normalized forward citations as

$$\widetilde{\text{fwcit}}_j = \frac{\text{fwcit}_j}{\overline{\text{fwcit}}_{p,t}}, \qquad \overline{\text{fwcit}}_{p,t} = \frac{1}{|S_{p,t}|} \sum_{j' \in S_{p,t}} \text{fwcit}_{j'},$$

where $S_{p,t}$ is the set of all semiconductor-related patents, from any country, filed at office p in year t. Each citation count is then expressed as a multiple of the office-year baseline. This normalization also absorbs first-order right-censoring in forward citations for recent filings: a patent filed in 2020 is expressed relative to other patents filed at the same office in 2020, all of which have had the same amount of time to accumulate citations.

High- and low-end semiconductor patents. A central question for semiconductor-control policy is whether technologically advanced semiconductors and related technologies are economically distinct from the rest. If downstream innovation depends disproportionately on high-end semiconductors and the technologies embodied in them, targeted controls on the technological frontier may be more effective than broad-based restrictions. Such targeting may be especially attractive when enforcement capacity is limited and controls entail foregone sales.

However, technological sophistication is inherently difficult to measure. Throughout our empirical analysis, we address this issue using two approaches. First, we treat the United States and its semiconductor-control-policy coalition allies as leaders at the semiconductor technological frontier. Accordingly, we classify as high-end those technology classes (IPC classes) in which the United States and its allies hold a technological advantage over China.[3] This measure of technological sophistication is outcome-based: it uses the current relative technological positions of countries that originate semiconductor innovation to identify high-end technology classes.

Our second complementary approach examines the distinction between high- and low-end technologies more directly, using text analysis of detailed patent documents. We apply this approach only in the firm-level analysis and therefore introduce it in Section B.8.[4]

[3] Section 4.1 defines the list of U.S. ally economies and explains how we measure the technology gap between the United States and its allies and China for each four-digit IPC technology class. Appendix B.4 explains the detailed construction of technology gap across semiconductor sectors between the U.S. and its allies versus China.

[4] This is because we have classified only semiconductor patents filed at the U.S. patent office by function and as high- or low-end using LLM text analysis, and the majority of these patents are therefore from U.S. firms (the classification

2.1 Impact of Semiconductor Tariffs on Downstream Innovation

2.1.1 Baseline Specification

We estimate the dynamic effects of upstream semiconductor trade shocks on downstream economic activity and innovation using local projections Jordà (2005). The unit of observation is an importer–downstream-sector–year cell, indexed by d, s, and t, respectively. Let $y_{dst} = g(Y_{dst})$, where $g(\cdot)$ denotes either the logarithmic or inverse-hyperbolic-sine transformation. Our primary outcome is innovation, measured by sectoral patent counts or citation-adjusted patent counts. For comparison, we also examine other outcomes, including aggregate assets, operating revenue, and employment. For each horizon h, we define the cumulative outcome relative to the year preceding the shock as

$$\Delta_h y_{s,d,t} \equiv y_{s,d,t+h} - y_{s,d,t-1}. \tag{2.1}$$

For $h = 0$, we suppress the time subscript and write $\Delta y \equiv y_t - y_{t-1}$. We estimate responses for horizons ranging from five years before to five years after the shock. We normalize the coefficient at $h = -1$ to zero and use the coefficients for $h = -5, \ldots, -2$ as pre-treatment placebo estimates.

$$\begin{aligned} \Delta_h y_{s,d,t} &= \beta_h \Delta x_{s,d,t} \\ &\quad + \mathbf{1}_{\{h \geq 0\}} \sum_{l=1}^{3} \rho_h^l \Delta y_{s,d,t-l} + \sum_{l=1}^{3} \theta_h^l \Delta x_{s,d,t-l} + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t+h}, \\ \text{where } x_{s,d,t-l} &\equiv \Gamma^{s,Semi} \sum_o \frac{\text{IMP}^{\text{Semi}}_{d,o,t_0}}{\text{Output}_{d,t_0}} \text{Tariff}^{\text{Semi}}_{d,o,t-l}. \end{aligned} \tag{2.2}$$

The specification includes destination–sector, destination–year, and sector–year fixed effects. We cluster standard errors at the destination–sector level and exclude semiconductor sectors from the downstream sample.

The change in exposure $\Delta x_{s,d,t}$. We set $t_0 = 1995$, the first year for which tariff data are available in our sample. $\text{IMP}^{\text{Semi}}_{d,o,t_0}$ denotes destination d's semiconductor imports from origin o in year t_0. Output_{d,t_0} denotes total output in destination-country d.[5]. The time-invariant coefficient $\Gamma^{s,Semi}$ captures downstream sector s's dependence on semiconductor inputs, based on the BEA input-output

task is ongoing). By contrast, our baseline patent regressions at the IPC-class level primarily exploit variation in semiconductor patents across origin countries. The firm-level analysis, in turn, contains substantially more variation across individual firms in their reliance on different compositions of semiconductor patent functions and in the technological sophistication of each function.

[5] We construct total destination-country output by aggregating firm-level output reported in ORBIS. We use this measure rather than official aggregate measures such as GDP to ensure consistency with outcome variables constructed using either ORBIS or ORBIS IP.

tables.

$\text{Tariff}^{\text{Semi}}_{d,o,t}$ denotes the corresponding bilateral applied tariff. We construct annual applied tariff rates on semiconductors for importing economies using the 1995–2023 WITS–TRAINS tariff files. For each importer, product, and year, we weight the WITS HS6 simple-average applied tariff rate by the number of underlying national tariff lines. We then aggregate across HS6 products to obtain an importer-year average semiconductor tariff rate.[6]

The lag structure. We include three lags of outcome growth, $\Delta y_{s,d,t-l}$, and three lags of the exposure shocks, $\Delta x_{s,d,t-l}$. Lagged outcome growth controls for persistence and mean reversion, helping to ensure that the coefficient on the current shock does not capture predictable outcome dynamics. We include lagged outcome controls only for $h \geq 0$, because lagged outcome growth mechanically overlaps with the dependent variable at negative horizons. Lagged exposure shocks account for serial correlation and the delayed effects of earlier shocks, separating the current tariff innovation from recent shock history. We select the lag length by comparing specifications with zero to three lags using the AIC and BIC in the $h = 0$ patent regression, estimated on a common sample. Both criteria favor three lags in the baseline specification. We then hold the selected lag order fixed across outcomes and horizons. Conditional on these lagged dynamics and the fixed effects, β_h captures the response to the current tariff shock rather than pre-existing outcome dynamics or previously accumulated shocks.

2.1.2 Instrumenting Applied Tariffs

To create exogenous variation for downstream sector's exposure to semiconductor tariff, we follow Boehm et al. (2023) and instrument applied tariff with applied MNF tariff. The idea is as follows. A country adjusts product MFN tariff mostly based on domestic need and negotiation with major trade partners. Hence, if the country applies MFN tariff to a smaller trade partner, and the MFN tariff is changed, such tariff change is likely exogenous to the country's trade relationship with the smaller trade partner. We define *Applied MFN Tariff* as follows:

$$\begin{aligned}\text{Applied MFN}^{\text{Semi}}_{d,o,t} = \text{MFN Tariff}^{\text{Semi}}_{d,t} &\times \mathbb{1}\{d \text{ applies MFN to } o\} \\ &\times \mathbb{1}\{o \text{ is not } d\text{'s top 5 trade partners}\},\end{aligned} \tag{2.3}$$

[6] A major part of semiconductor tariff changes are due to MFN tariff rates change coming from the WTO Information Technology Agreement. Our sample covers the periods of this agreement rolling out to more members, and we briefly introduce this agreement in Appendix Section B.5.

and define the instrument

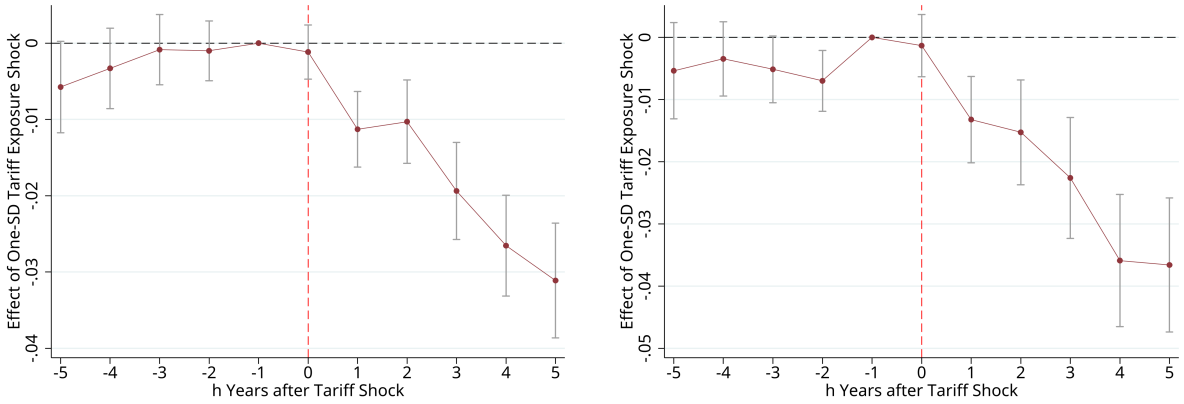
$$z_{s,d,t-l} \equiv \Delta \left[\Gamma^{s,Semi} \sum_{o} \frac{\text{IMP}^{\text{Semi}}_{d,o,t_0}}{\text{Output}_{d,t_0}} \text{Applied MFN}^{\text{Semi}}_{d,o,t-l} \right]. \tag{2.4}$$

We then jointly instrument the current shock and its three lags using $z_{s,d,t-l}$, for $l = 0, 1, 2, 3$.

2.1.3 Estimation Results

Figure 2.1 show the results for the outcome variable being the number of patents in the downstream sector, with both OLS and IV estimates. The OLS estimate suggests that a one-standard-deviation reduction in applied semiconductor tariff exposure is associated with a 3 percent increase in the number of patenting in five years on average for downstream sectors in the importing country. The IV estimates are even larger, and establish a nearly 4 percent causal effects of semiconductor tariff exposure reduction on downstream sector's innovation activity. In Appendix Figure B.1, we

Figure 2.1: Semiconductor Tariff Reduction Increases Downstream Patenting



(a) OLS (b) IV

Notes: The outcome variable is the number of patents. Panel (a) reports the one-standard-deviation effects estimated from Equation (2.2) in OLS. Panel (b) reports the corresponding one-standard-deviation IV estimate using (2.4). One SD refers to the exposure-weighted semiconductor tariff shock and is held fixed across outcomes and horizons. Points represent coefficient estimates, and error bars indicate 95% confidence intervals.

show that the effects are similarly large for total forward citations, and thus the innovation from more semiconductor inputs is not of lower quality. We also show corresponding estimates for other firm performance measures in Appendix Figure B.2, including total assets, operating revenue, and employees built from ORBIS. Interestingly, although we also see mostly positive effects from semiconductor tariff reductions, the effects are not as strong on patenting performance and seem to stabilize in two years and of much shorter impact. For robustness, we also repeat our exercises by

varying the set of controlled fixed effects and lagged variables. All our results remain robust and consistent with the baseline estimates.

2.2 Impact of Semiconductor Patents on Downstream Innovation

In this section, we exploit variation in upstream semiconductor patenting to examine its effects on downstream innovation, measured by downstream patents that cite semiconductor patents. Unlike tariff changes, citing a higher-quality semiconductor patent neither requires the purchase of semiconductor products nor entails a direct pecuniary cost. Our baseline specification is estimated at the sector level; we present complementary firm-level evidence in Appendix B.8.

For a downstream IPC sector s, destination country d, upstream semiconductor origin country o, and patent application year t, we estimate the same local-projection specification in (2.2), where s now denotes an IPC sector and the exposure measure is

$$x_{s,d,t} = \sum_{o} \frac{\text{Citation}^{\text{Semi}}_{s,d,o,t_0}}{\text{Citation}_{s,d,t_0}} \log\left(1 + \text{Patents}^{\text{Semi}}_{o,t}\right). \tag{2.5}$$

The exposure measure is constructed using the citation matrix and follows the network-exposure logic in Acemoglu et al. (2016a,b).

2.2.1 Instrumental Variable Estimation

To address the potential endogeneity of semiconductor patenting, we instrument U.S. semiconductor innovation using narrative shocks to U.S. federal nondefense public R&D appropriations constructed by Fieldhouse and Mertens (2024).[7] Define the U.S. and non-US origin semiconductor patent exposure, respectively: $x^{\text{US}}_{s,d,t} \equiv \frac{\text{Citation}^{\text{Semi}}_{s,d,US,t_0}}{\text{Citation}_{s,d,t_0}} \log\left(1 + \text{Patents}^{\text{Semi}}_{US,t}\right)$ and $x^{\text{non-US}}_{s,d,t} \equiv \sum_{o \neq US} \frac{\text{Citation}^{\text{Semi}}_{s,d,o,t_0}}{\text{Citation}_{s,d,t_0}} \log\left(1 + \text{Patents}^{\text{Semi}}_{o,t}\right)$. For each horizon $h = -5, \ldots, 5$, we estimate

$$\begin{aligned} \Delta_h y_{s,d,t} = & \sum_{o \in \text{US, non-US}} \beta^o_h \Delta x^o_{s,d,t} + \sum_{l=1}^{3} \sum_{o \in \text{US, non-US}} \theta^{l,o}_h \Delta x^o_{s,d,t-l} \\ & + \mathbf{1}_{\{h \geq 0\}} \sum_{l=1}^{3} \rho^l_h \Delta y_{s,d,t-l} + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t+h}. \end{aligned} \tag{2.6}$$

[7] Fieldhouse and Mertens (2024) construct the shock from major federal appropriations changes identified through legislative and historical records and unrelated to contemporaneous macroeconomic conditions. They show that positive nondefense R&D shocks increase US innovative activity and long-run productivity.

The US exposure term combines U.S. semiconductor patenting with the downstream cell's predetermined citation exposure to U.S. semiconductor knowledge. The non-US term controls for contemporaneous semiconductor innovation originating outside the U.S.

We treat U.S. semiconductor exposure as endogenous and instrument it with

$$\frac{\text{Citation}^{\text{Semi}}_{s,d,US,t_0}}{\text{Citation}_{s,d,t_0}}\xi^{RD}_{t-1}, \tag{2.7}$$

where ξ^{RD}_{t-1} is the lagged Fieldhouse–Mertens nondefense public R&D shock. The shock is identified from major changes in federal R&D appropriations that are unrelated to contemporaneous macroeconomic conditions. We interact it with each downstream cell's predetermined citation exposure to U.S. semiconductor innovation. The analysis therefore examines how U.S. semiconductor innovation affects downstream non-semiconductor innovation outside the United States.

Instrument relevance is supported by the positive response of U.S. semiconductor innovation to federal public R&D shocks. The first-stage coefficient is positive at every local-projection horizon, with horizon-specific F-statistics ranging from approximately 21.9 to 22.3. The exclusion restriction is supported by the narrative construction of the Fieldhouse–Mertens shock, which isolates federal R&D appropriations changes unrelated to contemporaneous macroeconomic conditions, and by the predetermined baseline citation weights. Destination–IPC, destination–year, and IPC–year fixed effects absorb persistent differences, country-specific shocks, and global technology trends. Controlling for non-U.S. semiconductor exposure further isolates the U.S. semiconductor-innovation channel from contemporaneous innovation elsewhere.

2.2.2 High- and Low-Ends Semiconductor Patents

Denote $g = H$ as high-end for the U.S.-and-its-allies-led semiconductor IPC main groups, and $g = L$ as low-end for the China-led semiconductor IPC main groups. And define the high- and low-end exposure: $x^{g}_{s,d,t-l} \equiv \sum_o \frac{\text{Citation}^{\text{Semi}}_{s,d,o,t_0}}{\text{Citation}_{s,d,t_0}} \log\left(1 + \text{Patents}^{\text{Semi},g}_{o,t-l}\right)$. For each horizon $h = -5, \ldots, 5$, we split the semiconductor innovation exposure into high- and low-end components:

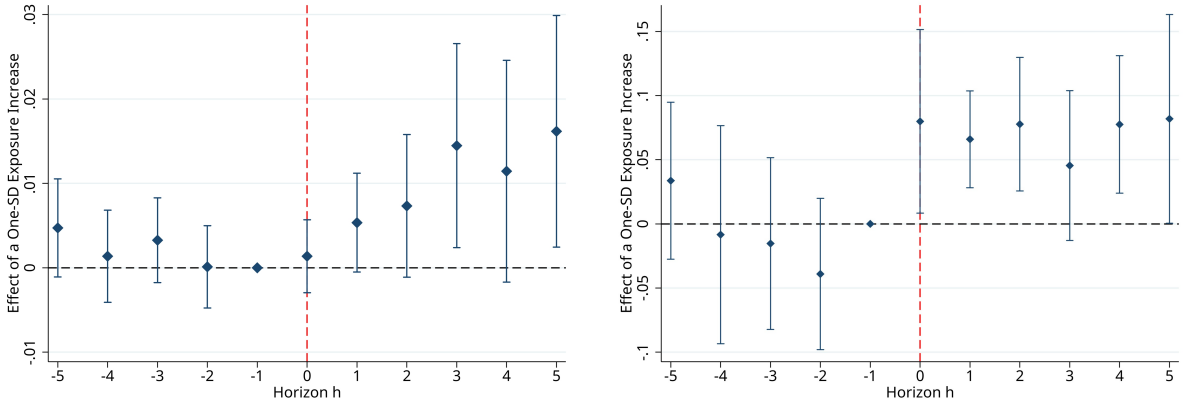
$$\begin{aligned}\Delta_h y_{s,d,t} = &\sum_{g=H,L} \beta^{g}_{h}\Delta x^{g}_{s,d,t} + \sum_{l=1}^{3}\sum_{g=H,L} \theta^{l,g}_{h}\Delta x^{g}_{s,d,t-l} \\ &+ \mathbf{1}_{\{h\geq 0\}}\sum_{l=1}^{3}\rho^{l}_{h}\Delta y_{s,d,t-l} + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t+h}.\end{aligned} \tag{2.8}$$

We estimate (2.8) using OLS.

2.2.3 Estimation Results

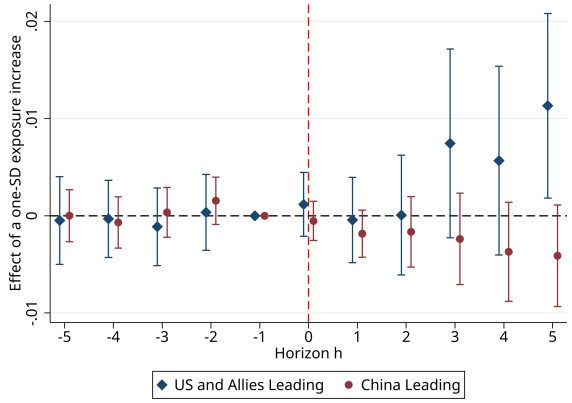
Figure 2.2 show the results for the outcome variable being the number of patents in the downstream sector. The OLS estimate suggests that a one-standard-deviation increase in semiconductor patent exposure is associated with about a 2-percent increase in the number of patenting in five years on average for downstream sectors in the importing country. Panel (c) shows that high-end semicon-

Figure 2.2: Semiconductor Tariff Reduction Increases Downstream Patenting



(a) OLS

(b) IV



(c) OLS: High- v.s. Low-end

Notes: Panel (a) reports the OLS estimated effects of a one-standard-deviation increase in aggregate semiconductor innovation exposure. Panel (b) reports the IV estimated effects of a one-standard-deviation increase in U.S.-origin semiconductor innovation exposure. Panel (c) reports the OLS estimated effects of a one-standard-deviation increase in both high- and low-end semiconductor innovation exposure. The error bars indicate 95% confidence intervals. The specification includes three lags of exposure growth at all estimated horizons and three lags of outcome growth when $h \geq 0$, together with destination-country–sector, destination-country–year, and sector–year fixed effects. Standard errors are clustered by destination-country–sector cell, and $h = -1$ is normalized to zero.

ductor patent exposure is the main reason for the positive association in Panel (a). The IV estimates in panel (b) are of much larger magnitudes, and suggest that a one-standard-deviation increase in

U.S.-origin semiconductor innovation exposure leads to about an 8-percent increase in downstream sector's patenting. For robustness, we also repeat our exercises by varying the set of controlled fixed effects and lagged variables. All our results remain robust and consistent with the baseline estimates.

3 Model

The economy is in continuous time over an infinite horizon and consists of two countries, indexed by $c \in \mathbb{C} = \{U \text{ (U.S.)}, C \text{ (China)}\}$. We examine both a stationary balanced growth path equilibrium and the transition dynamics between balanced growth paths.

The setup of the model is shown in Figure 3.1. Each country features a downstream sector and a semiconductor sector. Downstream firms produce tradable output and conduct R&D using semiconductors, which are aggregated from a continuum of varieties produced across both countries, subject to export controls. Semiconductor firms innovate strategically along a step-by-step quality ladder and compete oligopolistically. They innovate using downstream output, and, within each variety, a lagging firm can receive technology diffusion from the leader. A two-way general equilibrium linkage connects the two sectors: semiconductor prices and technological progress determine downstream innovation demand, while downstream semiconductor expenditures govern upstream market size and innovation incentives.

3.1 Model Setup

3.1.1 Representative Households

In period t, the households in each country $c \in \mathbb{C}$ maximize utility:

$$\max_{\{C_{c,s}\}} U_{c,t} \equiv \int_t^\infty \exp\left(-\rho\left(s-t\right)\right) \ln C_{c,s} ds, \tag{3.1}$$

subject to the flow budget constraint

$$P_{c,t}C_{c,t} + \dot{B}_{c,t} + \frac{\eta}{2}\left(B_{c,t} - \bar{B}_c\right)^2 = w_{c,t}L_c + w^S_{c,t}L^S_c + D_{c,t} + R_t B_{c,t} + \mathrm{Tr}_{c,t}, \tag{3.2}$$

where ρ is the discount factor, $C_{c,t}$ is the consumption of final good, $P_{c,t}$ is the price of final good, $B_{c,t}$ denotes the stock of internationally traded risk-free bonds yielding an instantaneous net interest rate R_t, $\dot{B}_{c,t}$ denotes the net accumulation of these bonds, $\bar{B}_c$ denotes steady state bond holdings,

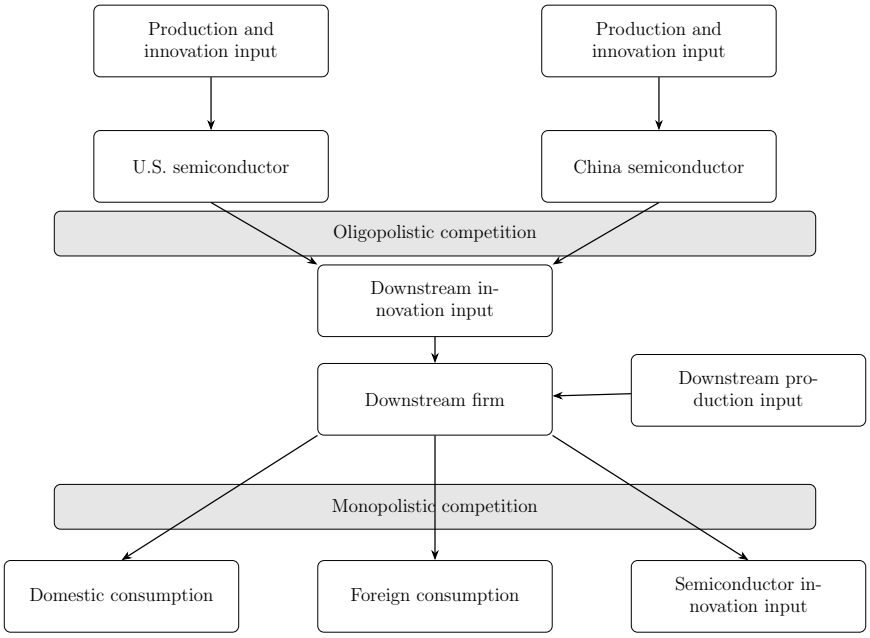


Figure 3.1: Model Environment

Notes: This figure shows the model environment: countries, sectors, production and innovation input–output relationship, and market structures.

and $\eta > 0$ indicates quadratic adjustment cost of international portfolios to ensure unique steady state solution (cf. Schmitt-Grohe and Uribe 2003).

L_c and L_c^S denote the labor supply of downstream goods and semiconductors, respectively. Labor is immobile across countries and sectors. Sector-specific labor supply is considered, as the data show that semiconductor-related workers account for a limited labor supply in the total economy and earn a different wage rate. $w_{c,t}$ and $w_{c,t}^S$ denote the wage rate for each type of labor supply. $D_{c,t}$ is net dividends after firms pay semiconductor inputs and innovation costs. The utility maximization problem leads to a standard Euler equation. See detailed derivations in Appendix A.1.1.

3.1.2 Final Goods

Final output $Y_{c,t}$ in country c is used for consumption, production, and innovation inputs. It combines downstream outputs $y_{c'c,t}$ from countries $c' \in \mathbb{C}$ according to:

$$Y_{c,t} = \left(\sum_{c' \in \mathbb{C}} (y_{c'c,t})^{\frac{\sigma-1}{\sigma}} \right)^{\frac{\sigma}{\sigma-1}}, \tag{3.3}$$

where $\sigma > 1$ represents the elasticity of substitution across downstream goods. Final good producers operate competitively. Their profit maximization gives the following demand for downstream output:

$$y_{c'c,t} = \left(\frac{d_{c'c}p_{c',t}}{P_{c,t}}\right)^{-\sigma} Y_{c,t}, \tag{3.4}$$

where the final good price is given by:

$$P_{c,t} = \left(\sum_{c' \in \mathbb{C}} \left(d_{c'c}p_{c',t}\right)^{1-\sigma}\right)^{\frac{1}{1-\sigma}}, \tag{3.5}$$

$p_{c',t}$ denotes the price of downstream output and $d_{c'c} \geq 1$ denotes the downstream trade costs from country c' to country c.

3.1.3 Downstream Goods Production

A representative downstream good producer in country c employs labor $l_{c,t}$ to produce output $y_{c,t}$:

$$y_{c,t} = z_{c,t}^{\frac{1}{\sigma-1}} l_{c,t}, \tag{3.6}$$

The firm sells output to final good producers in all countries subject to trade costs: $y_{c,t} = \sum_{c' \in \mathbb{C}} d_{cc'} y_{cc',t}$. Downstream firms engage in monopolistic competition. Their profit maximization problem yields a constant markup over marginal cost. We denote the profits of downstream firms selling from country c to c' by $\pi_{cc',t}$ and the sum of profits across all destination markets by $\Pi_{c,t} = \sum_{c' \in \mathbb{C}} \pi_{cc',t}$. Explicit formulas are detailed in Appendix A.1.2.

3.1.4 Downstream Innovation

The representative downstream firm in country c uses semiconductors $Y_{c,t}^S$ to increase its productivity. Downstream productivity evolves according to:

$$\dot{z}_{c,t} = \iota_c\left(\bar{z}_t - z_{c,t}\right) \; + \; \lambda_c^d \left(Y_{c,t}^S\right)^{\alpha} z_{c,t}^{1-\alpha}, \tag{3.7}$$

where $\bar{z}_t$ denote the aggregate world technology stock, which individual firms take as given. The parameter $\iota_c \in [0, 1]$ governs the extent of knowledge diffusion from this global frontier, generating international spillovers that enable all countries to share a common growth rate along the balanced growth path.

The parameter λ_c^d represents downstream innovation efficiency. $\alpha \in (0, 1)$ dictates the intensity

of semiconductors in downstream innovation. Allowing λ_c^d to be country-specific generates cross-country differences in baseline productivity levels. In contrast, α is uniform across countries, reflecting the universal nature of innovation technology.

Downstream Firm Value Function. The maximization problem of the downstream firm is as follows:

$$R_t V_{c,t} - \dot{V}_{c,t} = \max_{Y_{c,t}^S} \left\{ \Pi_{c,t} - P_{c,t}^S (1-\kappa_c) Y_{c,t}^S + \frac{\partial V_{c,t}}{\partial z_{c,t}} \dot{z}_{c,t} \right\}, \tag{3.8}$$

where $V_{c,t}$ denotes the value of the downstream producer, $\dot{V}_{c,t} = \frac{\partial V_{c,t}}{\partial t}$ denotes the derivative of $V_{c,t}$ with respect to time, $P_{c,t}^S$ denotes semiconductor price, and κ_c denotes innovation subsidy to downstream innovation. The downstream demand for semiconductors equals the following:

$$Y_{c,t}^S = z_{c,t} \left(\frac{\alpha \lambda_c^d \frac{\partial V_{c,t}}{\partial z_{c,t}}}{(1-\kappa_c) P_{c,t}^S} \right)^{\frac{1}{1-\alpha}}. \tag{3.9}$$

Semiconductor demand is decreasing in price $P_{c,t}^S$ and increasing in the marginal benefit of productivity $\frac{\partial V_{c,t}}{\partial z_{c,t}}$, innovation efficiency λ_c^d, input elasticity α, the innovation subsidy κ_c, and domestic productivity $z_{c,t}$. The detailed derivations for the downstream firms' innovation problem both on the BGP and in transitions are in Appendix A.1.10, A.1.11.

3.1.5 Semiconductor Production

The aggregate semiconductor input $Y_{c,t}^S$ combines a unit continuum of varieties $Y_{c,t}^S(\omega)$, indexed by $\omega \in [0,1]$, according to:

$$Y_{c,t}^S = \exp\left(\int_0^1 \ln \left[Y_{c,t}^S(\omega) \right] d\omega \right). \tag{3.10}$$

Within each semiconductor variety ω, one domestic firm and one foreign firm engage in oligopolistic competition. Using foreign-produced semiconductors not only results in variety gains, but also in efficiency gains (higher supply and lower price). The variety-level output $Y_{c,t}^S(\omega)$ combines their outputs with an elasticity of substitution σ^S:

$$Y_{c,t}^S(\omega) = \left(\sum_{c' \in \mathbb{C}} 1_{c'c}^{\text{export}}(\omega) \cdot \left[y_{c'c,t}^S(\omega) \right]^{\frac{\sigma^S - 1}{\sigma^S}} \right)^{\frac{\sigma^S}{\sigma^S - 1}}, \ \sigma^S > 1. \tag{3.11}$$

$1^{\text{export}}_{c'c}(\omega)$ denotes the variety-specific export control policy:

$$1^{\text{export}}_{c'c}(\omega) = \begin{cases} 0, & \text{if exporting from } c' \text{ to } c \text{ for variety } \omega \text{ is banned,} \\ 1, & \text{if exporting from } c' \text{ to } c \text{ for variety } \omega \text{ is allowed.} \end{cases} \tag{3.12}$$

A semiconductor firm in country c with productivity $z^S_{c,t}(\omega)$ operates a production technology linear in semiconductor labor $l^S_{c,t}(\omega)$:

$$y^S_{c,t}(\omega) = z^S_{c,t}(\omega) l^S_{c,t}(\omega), \tag{3.13}$$

Taking other producers' quantities as given, semiconductor intermediate producers choose output and labor input to maximize profits in each destination market, subject to trade policies, production technology, and demand from semiconductor aggregate-good producers. This yields the following markup pricing rule in each destination market $c' \in C$:

$$p^S_{cc',t}(\omega) = \frac{\varepsilon_{cc',t}(\omega)}{\varepsilon_{cc',t}(\omega) - 1} \frac{w^S_{c,t}}{z^S_{c,t}(\omega)}, \tag{3.14}$$

where the demand elasticity is given by

$$\varepsilon_{cc',t}(\omega) \equiv s^S_{cc',t}(\omega) + \sigma^S \left(1 - s^S_{cc',t}(\omega)\right), \tag{3.15}$$

where $s^S_{cc',t}(\omega)$ denotes the market share of country c's variety semiconductor firm in country c'.

Consistent with previous literature (e.g., Atkeson and Burstein 2008), semiconductor firms' pricing and production decisions depend solely on the *relative productivity* across countries within each intermediate variety ω. A higher relative productivity lowers a firm's relative price while expanding its market share, markup, output, and operating profits, thereby strengthening incentives to innovate and establish technological leadership.

The price of semiconductor variety ω in country c equals the following ($d^S_{cc',t} \geq 1$ denotes iceberg trade costs for semiconductors):

$$P^S_{c,t}(\omega) = \left(\sum_{c' \in \mathbb{C}} 1^{\text{export}}_{c'c}(\omega) \cdot \left[d^S_{c'c} p^S_{c'c,t}(\omega) \right]^{1-\sigma^S} \right)^{\frac{1}{1-\sigma^S}}. \tag{3.16}$$

Together with the pricing rule $p^S_{cc'}(\omega)$, it determines a firm's market share, and thus profit $\pi^S_{cc'}(\omega)$ in market c'. We show that the total semiconductor operating profits for a semiconductor from c can be written as $\Pi^S_{c,t}(\omega) P^S_{c,t} Y^S_{c,t}$, where $\Pi^S_{c,t}(\omega)$ depends on its market shares and markups in

both markets (thus is determined by its technology gap with its competitor and its accessibility to the two markets), and $P^S_{c,t}$ is the aggregate semiconductor price in country c (thus $P^S_{c,t}Y^S_{c,t}$ is the total market size). This total operating profit enters the semiconductor producer's HJB, and shows explicitly that semiconductor profits are determined by technology-gap-dependent market shares and markups, destination semiconductor expenditures, and market access. The detailed derivations for the downstream firms' innovation problem both on the BGP and in transitions are in Appendix A.1.3.

3.1.6 Semiconductor Innovation

Semiconductor firms innovate along a quality ladder to advance their productivity. A firm in country c producing variety ω at time t possesses productivity $z^S_{c,t}(\omega) \equiv \lambda^{k_{c,t}(\omega)}$, where $k_{c,t}(\omega) \in \mathbb{N}$ denotes the firm's technological rung and $\lambda > 1$ represents the step size of quality improvements. The relative productivity between country U and country C is given by $\frac{z^S_{U,t}(\omega)}{z^S_{C,t}(\omega)} = \lambda^{k_{U,t}(\omega)-k_{C,t}(\omega)}$.

We use the bilateral technology gap as the state variable. Defining $m_t(\omega) \equiv k_{U,t}(\omega) - k_{C,t}(\omega)$, variety ω is classified as U.S.-led if $m_t(\omega) > 0$, China-led if $m_t(\omega) < 0$, and neck-and-neck if $m_t(\omega) = 0$. Because firm decisions depend only on relative productivity, each variety can be indexed directly by its state m. For computational tractability, the state space is bounded such that $m \in \{-\bar{m}, \dots, 0, \dots, \bar{m}\}$. We define the variety-level semiconductor frontier by:

$$K^F_t(\omega) \equiv \max\{k_{U,t}(\omega), k_{C,t}(\omega)\}, \qquad a^F_t(\omega) \equiv \lambda^{K^F_t(\omega)}. \tag{3.17}$$

The country-specific semiconductor productivity of a variety can be written as

$$z^S_{U,t}(\omega) = A^F_t \widehat{z}^S_U(m_t(\omega)), \qquad \widehat{z}^S_U(m) \equiv \lambda^{\min\{m,0\}}, \tag{3.18}$$

$$z^S_{C,t}(\omega) = A^F_t \widehat{z}^S_C(m_t(\omega)), \qquad \widehat{z}^S_C(m) \equiv \lambda^{-\max\{m,0\}}. \tag{3.19}$$

The aggregate world semiconductor frontier is the geometric mean

$$A^F_t \equiv \exp\left(\int_0^1 \log a^F_t(\omega) d\omega\right). \tag{3.20}$$

The semiconductor production uses the relative productivities $\widehat{z}^S_o(m)$ and the detrended semiconductor prices $\widehat{p}^S_{od,t}(m) \equiv a^F_t(\omega) p^S_{od,t}(\omega)$ at the variety level and $\widehat{P}^S_{d,t} \equiv A^F_t P^S_{d,t}$ at the aggregate level.

Semiconductor producers' innovations follow a controlled Poisson process, with the arrival rate

$e_{c,t}(m)$ determined by their innovation investment

$$RD^S_{c,t}(m) = \frac{\lambda^s_c(1-\kappa^s_c)}{\gamma} e_{c,t}(m)^\gamma Q^S_{c,t}, \tag{3.21}$$

where $\lambda^s_c > 0$ represents the scale of semiconductor innovation cost, $\gamma > 1$ implies innovation investment is convex in the arrival rate, and κ^s_c denotes the innovation subsidy, a common policy in semiconductor industry across countries (cf. Goldberg et al. (2024)).[8] The semiconductor innovation shifter is normalized by the world semiconductor frontier:

$$Q^S_{c,t} \equiv (A^F_t)^{1/(\sigma-1)}. \tag{3.22}$$

On a BGP with $A^F_t = A^F_0 \exp(g^S t)$, this implies $Q^S_{c,t} = (A^F_0)^{1/(\sigma-1)} \exp(g^S t/(\sigma-1))$. $Q^S_{c,t}$ represents that the innovation investment is priced by final goods and is increasing along the balanced growth path, such that $P_{c,t}Q^S_{c,t}$ and $P_{c,t}RD^S_{c,t}(m)$ are stationary along the balanced growth path.

Countries that are not in the global technology frontier also improve their productivity by getting knowledge spillovers from the global frontier. The knowledge spillovers across countries exist to ensure the existence of a non-degenerate equilibrium along the balanced growth path. Within a time interval Δt, country U receives knowledge spillovers freely with probability

$$\iota(m, 1_{C \text{ exports to } U}) = \begin{cases} \epsilon & \text{if} \quad 1_{C \text{ exports to } U} = 0 \quad \text{and} \quad m < 0, \\ \iota^S & \text{if} \quad 1_{C \text{ exports to } U} = 1 \quad \text{and} \quad m < 0, \\ 0 & \text{if} \quad m \geq 0, \end{cases}$$

and country C receives knowledge spillovers freely with probability

$$\iota(m, 1_{U \text{ exports to } C}) = \begin{cases} \epsilon & \text{if} \quad 1_{U \text{ exports to } C} = 0 \quad \text{and} \quad m > 0, \\ \iota^S & \text{if} \quad 1_{U \text{ exports to } C} = 1 \quad \text{and} \quad m > 0, \\ 0 & \text{if} \quad m \leq 0, \end{cases}$$

where $\epsilon > 0$ is arbitrarily small ($\epsilon \ll \iota^S$) and ensures the existence of a non-degenerate equilibrium.

The knowledge diffusion margin is particularly relevant for semiconductors. Frontier semiconductor technology is not just embodied in a single blueprint or machine. It accumulates through learning-by-doing and close interactions among chip designers, foundries, equipment suppliers, customers, and engineers, and it crosses borders through foreign direct investment, research collab-

[8] The specification implies that within a time interval Δt, the probability of an innovation occurring is $e_{c,t}(m)\Delta t + o(\Delta t)$, and the probability of more than one innovation arriving is $o(\Delta t)$.

orations, technology licensing, worker mobility, and customer–supplier relationships.[9]

We use a function $F_c(m, m')$ to summarize the productivity change due to innovation or getting knowledge spillovers. We consider a special case: productivity can only increase by λ so that the technology gap changes step by step, motivated by previous literature (cf. Sui (2023)). Since $m = k_U - k_C$, successful innovation by country U raises m by one step to $m' = m + 1$, while successful innovation by country C lowers m by one step to $m' = m - 1$. Therefore, the transition function is country-specific:

$$F_U(m, m') = \begin{cases} 1 & \text{if } m' = \min\{m+1, \bar{m}\}, \\ 0 & \text{otherwise.} \end{cases} \qquad F_C(m, m') = \begin{cases} 1 & \text{if } m' = \max\{m-1, -\bar{m}\}, \\ 0 & \text{otherwise.} \end{cases} \tag{3.23}$$

Given others' decisions, the value function of firms in country c satisfies:

$$\begin{aligned} R_t V^S_{c,t}(m) - \dot{V}^S_{c,t}(m) = \max_{e_{c,t}(m)\in[0,\bar{e}]} \{ & \Pi^S_{c,t}(m) P^S_{c,t} Y^S_{c,t} - P_{c,t} R D^S_{c,t}(m) \\ & + (e_{c,t}(m) + \iota(m, 1_{c' \text{ exports to } c}))[\sum_{m'} F_c(m, m') V^S_{c,t}(m') - V^S_{c,t}(m)] \\ & + (e_{c',t}(m) + \iota(m, 1_{c \text{ exports to } c'}))[\sum_{m'} F_{c'}(m, m') V^S_{c,t}(m') - V^S_{c,t}(m)], \end{aligned} \tag{3.24}$$

where $V^S_{c,t}(m)$ denotes the value of semiconductor intermediate producer in country c with technology gap m at period t, $\dot{V}^S_{c,t}(m)$ denotes the derivative of $V^S_{c,t}(m)$ with respect to time, $\Pi^S_{c,t}(m) P^S_{c,t} Y^S_{c,t}$ denotes the optimal production profit of this semiconductor intermediate producer, and $\Pi^S_{c,t}(m)$ is specified in equation (A.16). This results in the following optimal innovation decision:

$$e_{c,t}(m) = \left(\frac{[\sum_{m'} F_c(m, m') V^S_{c,t}(m') - V^S_{c,t}(m)]}{\lambda^s_c (1 - \kappa^s_c) P_{c,t} Q^S_{c,t}} \right)^{\frac{1}{\gamma - 1}}. \tag{3.25}$$

3.2 Equilibrium

In this section, we define the balanced growth path equilibrium and key variables of interest.

[9] Goldberg et al. (2024) show that access to foreign technology was historically central to the emergence of semiconductor industries in follower countries and find strong cross-border learning spillovers. They also emphasize that these spillovers depend on deliberate commercial and research relationships and can therefore be curtailed by excluding a country from frontier technology.

3.2.1 Equilibrium Definition

A Balanced Growth Path (BGP) Equilibrium of the two-country economy consists of prices $\{R_t, w_{c,t}, w^S_{c,t}, P^S_{c,t}, P_{c,t}, p^S_{cc',t}(m), p_{c,t}\}$, and allocations $\{Y^S_{c,t}, Y_{c,t}, C_{c,t}, l_{c,t}, l^S_{c,t}(m), y_{c'c,t}, y^S_{cc',t}(m), e_{c,t}(m), \mu_t(m), z_{c,t}, B_{c,t}\}$ such that for $c \in \mathbb{C}$, $m \in \{-\bar{m}, ..., 0, ..., \bar{m}\}$ and all $t \in [0, \infty)$,
(i) households choose $C_{c,t}$ to maximize utility subject to budget constraints, pinning down R_t;
(ii) final good producers optimize profits to buy downstream intermediate goods $y_{c'c,t}$;
(iii) downstream intermediate goods producers choose $p_{c,t}$, $l_{c,t}$, $Y^S_{c,t}$ to solve their pricing, employment, and semiconductor input usage decisions;
(iv) semiconductor aggregate good producers optimize profits to buy intermediates $y^S_{cc',t}(m)$;
(v) semiconductor intermediate producers choose $p^S_{cc',t}(m)$, $l^S_{c,t}(m)$, and $e_{c,t}(m)$ to solve their pricing, employment and innovation decision;
(vi) final good market clears in each country:

$$C_{c,t} = Y_{c,t} - \sum_m RD^S_{c,t}(m)\mu_t(m); \tag{3.26}$$

(vii) downstream labor market clears in each country ($w_{U,t} \equiv 1$):

$$w_{c,t}L_c = w_{c,t}l_{c,t} = \frac{\sigma - 1}{\sigma} \sum_{c' \in \mathbb{C}} s_{cc',t}P_{c',t}Y_{c',t}; \tag{3.27}$$

(viii) semiconductor labor market clears in each country:

$$w^S_{c,t}L^S_c = \sum_{c' \in \mathbb{C}} \sum_m \frac{\varepsilon_{cc',t}(m) - 1}{\varepsilon_{cc',t}(m)} s^S_{cc',t}(m)P^S_{c',t}Y^S_{c',t}\mu_t(m); \tag{3.28}$$

(ix) the bond market clears:

$$\sum_{c \in \mathbb{C}} B_{c,t} = 0, \tag{3.29}$$

$B_{c,t} = \bar{B}_c$, where $\bar{B}_c$ is exogenously given to pin down steady state bond holdings;
(x) balance of payments hold:

$$EX_{cc',t} - EX_{c'c,t} + EX^S_{cc',t} - EX^S_{c'c,t} + R_tB_{c,t} - \dot{B}_{c,t} = 0, \tag{3.30}$$

where $\text{EX}_{cc',t} = s_{cc',t}P_{c',t}Y_{c',t}$; $\text{EX}^S_{cc',t} = P^S_{c',t}Y^S_{c',t} \sum_m s^S_{cc',t}(m)\mu_t(m)$.
(xi) downstream productivity evolves according to equation (3.7), ensuring a downstream productivity $z_{c,t}$ that is consistent with downstream firms' decisions;

(xii) relative productivity in the semiconductor sector evolves according to equation (A.86), ensuring a stationary distribution of firms over semiconductor technology gaps $\mu_t(m)$;
and (xiii) on a BGP, downstream productivity growth is equal to semiconductor productivity growth, and the growth rates of all variables are specified in Appendix A.1.

3.2.2 Technology Advantage

Define the U.S. semiconductor technology advantage over China as

$$\text{S Tech Advantage}_t \equiv \sum_m m \cdot \mu_t(m) = \frac{\log A^S_{U,t} - \log A^S_{C,t}}{\log \lambda}, \tag{3.31}$$

where m represents the technology gap between U and C and $\mu_t(m)$ represents the distribution of semiconductor firms over the technology gap. $A^S_{U,t}$ and $A^S_{C,t}$ are country-level semiconductor productivity indices, defined in equations (A.22) and (A.23).

Define the U.S. downstream technology advantage over China as

$$\text{D Tech Advantage}_t \equiv z_{U,t}/z_{C,t}, \tag{3.32}$$

where $z_{c,t}$ represents the level of downstream productivity in country $c \in \{U, C\}$.

3.2.3 Growth

As shown by Proposition 3.1, along the BGP, both countries' aggregate semiconductor growth grow at the same rate, and the semiconductor price $P^S_{c,t}$ declines at the same rate.

Proposition 3.1 (Semiconductor growth) *Let $\lambda > 1$ be the semiconductor step size and let $\mu(m)$ be the stationary distribution of technology gaps $m = k_U - k_C$. The common semiconductor productivity growth rate on the BGP is*

$$g^S = \left[\sum_{m>0} e_U(m)\mu(m) + \sum_{m<0} e_C(m)\mu(m) + (e_U(0) + e_C(0))\,\mu(0)\right] \ln(\lambda). \tag{3.33}$$

Moreover,

$$g_{Z^S_U} = g_{Z^S_C} = g^S, \qquad g_{P^S_c} = -g^S, \qquad g_{Y^S_c} = g^S, \qquad g_{P^S_c Y^S_c} = g_{w^S_c} = 0. \tag{3.34}$$

Here g^S is the growth rate of the absolute world semiconductor frontier A^F_t.

Proof: See Appendix A.1.8.

Let g^d denote the BGP growth rate of downstream productivity $z_{c,t}$, and define the downstream innovation intensity $u_c \equiv Y^S_{c,t}/z_{c,t}$. Proposition 3.2 shows that a BGP with stationary relative downstream productivities and stationary semiconductor expenditure requires semiconductor and downstream productivity to grow at the same rate.

Proposition 3.2 (Downstream growth, common growth, and feasibility) *On an interior BGP with strictly positive and stationary u_c, downstream productivity growth equals semiconductor productivity growth:*

$$g^d = g^S \equiv g. \tag{3.35}$$

Equivalently, the relative downstream productivity $\widehat{z}_{c,t} = z_{c,t}/A^F_t$ is stationary on the BGP:

$$\frac{\dot{\widehat{z}}_{c,t}}{\widehat{z}_{c,t}} = 0, \qquad \frac{\dot{z}_{c,t}}{z_{c,t}} = \frac{\dot{A}^F_t}{A^F_t} = g^S. \tag{3.36}$$

The downstream growth condition in country c is

$$g = \iota_c \left(\frac{\bar{z}_t}{z_{c,t}} - 1 \right) + \lambda^d_c u^\alpha_c. \tag{3.37}$$

With fixed labor supplies and stationary relative wages and productivity ratios, the other BGP growth rates are

$$g_{w_c} = 0, \qquad g_{s_{cc'}} = 0, \qquad g_{P_c} = -\frac{g}{\sigma - 1}, \qquad g_{Y_c} = g_{C_c} = \frac{g}{\sigma - 1}, \qquad g_{P_c Y_c} = g_{\Pi_c} = g_{EX_{cc'}} = 0. \tag{3.38}$$

In the two-country case with $\bar{z}_t = z_{U,t} + z_{C,t}$ and $r^d \equiv z_U/z_C$, an interior BGP must satisfy

$$g > \frac{\iota_U}{r^d}, \qquad g > \iota_C r^d, \qquad g^2 > \iota_U \iota_C. \tag{3.39}$$

If $\iota_U = \iota_C = \iota$, the necessary condition to ensure an interior BGP reduces to $\iota < g$.
Proof: See Appendix A.1.13.

3.2.4 Welfare

Welfare is measured by discounted sum of utility over time at time zero in each country. Specifically, the welfare of country c over horizon T at time t is

$$W_{c,t} = \int_t^{t+T} \exp(-\rho(s-t)) \log(C_{c,s}) ds. \tag{3.40}$$

We present the welfare effect of U.S. semiconductor control (or more generally, the differences in welfare between a counterfactual and the baseline economy) in consumption equivalent terms as:

$$\int_t^{t+T} \exp(-\rho(s-t)) \log(C_{c,s}^{new}) ds = \int_t^{t+T} \exp(-\rho(s-t)) \log\left((1+\varsigma) C_{c,s}^{base}\right) ds. \tag{3.41}$$

This equation explains that if U.S. semiconductor control at time t generates a new consumption path C_{cs}^{new} between t and $t+T$, it leads to a ς % variation in consumption-equivalent welfare over the horizon T. In other words, it results in a ς % increase in consumption at each point in time between t and $t+T$. We study the welfare change in both the transition and the new BGP as $T \to \infty$.

3.3 Model Mechanism: Interplay between Semiconductor and Downstream

This section characterizes the feedback loop between semiconductors and downstream innovation. The model has two core links. First, semiconductor prices determine downstream semiconductor demand and hence downstream productivity growth. Second, downstream semiconductor expenditures determine the market size and profits of semiconductor producers, which feed back into strategic semiconductor innovation. Export controls affect growth by moving both links through market clearing, prices, and technology-gap-dependent firm values.

3.3.1 Semiconductor Innovation

Using $E_{c,t}^S \equiv P_{c,t}^S Y_{c,t}^S$ and $v_{c,t}^S(m) \equiv V_{c,t}^S(m)/E_{c,t}^S$, the semiconductor innovation FOC in (3.25) can be written as

$$e_{c,t}(m) = \left(\frac{\Delta v_{c,t}^S(m) E_{c,t}^S}{\lambda_c^S (1-\kappa_c^S) P_{c,t} Q_{c,t}^S} \right)^{\frac{1}{\gamma-1}}, \qquad \Delta v_{c,t}^S(m) \equiv \sum_{m'} F_c(m,m') v_{c,t}^S(m') - v_{c,t}^S(m). \tag{3.42}$$

Log-linearizing (3.42) gives

$$\widehat{e}_{c,t}(m) = \frac{1}{\gamma - 1}\left[\widehat{E}^S_{c,t} + \widehat{\Delta v}^S_{c,t}(m) - \widehat{P}_{c,t} - \widehat{Q}^S_{c,t} - \widehat{\lambda}^S_c - \widehat{(1-\kappa^S_c)}\right]. \tag{3.43}$$

Thus semiconductor innovation depends on four objects: semiconductor market size $E^S_{c,t}$; the final-good cost of semiconductor R&D $P_{c,t}Q^S_{c,t}$; innovation-cost and subsidy shifters λ^S_c and κ^S_c; and the strategic innovation prize $\Delta v^S_{c,t}(m)$.

Semiconductor market size effect. The semiconductor labor market clearing condition is

$$w^S_{c,t}L^S_c = \sum_{c' \in \mathbb{C}} \sum_m \frac{\varepsilon_{cc',t}(m) - 1}{\varepsilon_{cc',t}(m)} s^S_{cc',t}(m) E_{c',t}\mu_t(m). \tag{3.44}$$

For fixed productivities and markups, a decline in $w^S_{c,t}$ lowers semiconductor intermediate prices and therefore lowers the aggregate semiconductor price $P^S_{d,t}$ in destinations where country c is an active supplier. When export controls reduce foreign sales, the fall in semiconductor labor demand can reduce $w^S_{c,t}$ and stimulate domestic downstream semiconductor absorption. Whether $E^S_{c,t}$ rises or falls depends on whether the domestic demand expansion is large enough to offset the lost foreign market.

Downstream semiconductor-demand elasticity. The downstream FOC (3.9) implies

$$\ln Y^S_{c,t} = \ln z_{c,t} + \frac{1}{1-\alpha}\left[\ln(\alpha\lambda^d_c) + \ln\left(\frac{\partial V_{c,t}}{\partial z_{c,t}}\right) - \ln(1-\kappa_c) - \ln P^S_{c,t}\right]. \tag{3.45}$$

Holding $z_{c,t}$ and $\partial V_{c,t}/\partial z_{c,t}$ fixed,

$$\frac{\partial \ln Y^S_{c,t}}{\partial \ln P^S_{c,t}} = -\frac{1}{1-\alpha}, \qquad \frac{\partial \ln E^S_{c,t}}{\partial \ln P^S_{c,t}} = -\frac{\alpha}{1-\alpha}. \tag{3.46}$$

Because $\alpha \in (0,1)$, semiconductor demand is price elastic and semiconductor expenditure rises when $P^S_{c,t}$ falls, holding the dynamic marginal value fixed. In general equilibrium,

$$\frac{d \ln Y^S_{c,t}}{d \ln P^S_{c,t}} = -\frac{1}{1-\alpha} + \frac{1}{1-\alpha}\frac{d \ln(\partial V_{c,t}/\partial z_{c,t})}{d \ln P^S_{c,t}} + \frac{d \ln z_{c,t}}{d \ln P^S_{c,t}}, \tag{3.47}$$

so the total response also depends on how cheaper semiconductors change future productivity and the marginal value of additional productivity.

Downstream input cost effect. Equation (A.10) implies that higher downstream productivity lowers the final-good price:

$$P_{c,t} = \left(d_{cc} \frac{\sigma}{\sigma - 1} \frac{w_{c,t}}{z_{c,t}^{\frac{1}{\sigma-1}}} \right) \left[1 + \sum_{k \neq c} \left(\frac{d_{kc} w_{k,t}}{d_{cc} w_{c,t}} \right)^{1-\sigma} \frac{z_{k,t}}{z_{c,t}} \right]^{\frac{1}{1-\sigma}}. \tag{3.48}$$

Since semiconductor R&D is paid in final-good units, a lower $P_{c,t}$ reduces $P_{c,t} Q_{c,t}^S$ in (3.42) and raises semiconductor innovation incentives.

Strategic spillover and escape-competition channel. The strategic innovation prize is

$$\Delta_{c,t}^S(m) \equiv \sum_{m'} F_c(m, m') V_{c,t}^S(m') - V_{c,t}^S(m). \tag{3.49}$$

An export control that reduces foreign spillovers changes this prize even if market size is held fixed. In a local two-state approximation for a U.S. firm that can become a leader rather than remain neck-and-neck, let $\pi_L - \pi_N > 0$ be the flow leadership advantage and let r be the effective discount rate. If Chinese catch-up erodes the U.S. lead at rate $e_C + \iota^S$ under open trade and at rate $e_C + \epsilon$ under the export control, with $0 < \epsilon \ll \iota^S$, then

$$\Delta_U^{open} = \frac{\pi_L - \pi_N}{r + e_C + \iota^S}, \qquad \Delta_U^{ban} = \frac{\pi_L - \pi_N}{r + e_C + \epsilon}, \qquad \Delta_U^{ban} > \Delta_U^{open}. \tag{3.50}$$

Combining this with (3.42), U.S. semiconductor innovation rises after the export control if and only if

$$\frac{E_U^{S,ban}}{E_U^{S,open}} \frac{\Delta v_U^{S,ban}(m)}{\Delta v_U^{S,open}(m)} \frac{P_U^{open} Q_U^{S,open}}{P_U^{ban} Q_U^{S,ban}} > 1. \tag{3.51}$$

Equation (3.51) clarifies the short-run boom/long-run bust mechanism. In the short run, the spillover reduction raises the strategic prize and lower domestic semiconductor prices can raise E_U^S. In the long run, if the U.S. becomes sufficiently far ahead, the escape-competition prize can shrink and the lost Chinese market can dominate, lowering $E_U^S \Delta v_U^S(m)$.

3.3.2 Downstream Innovation

The downstream block converts semiconductor prices into downstream productivity growth. Combining (A.106) and (3.45), a decline in $P_{c,t}^S$ raises $u_{c,t} = Y_{c,t}^S / z_{c,t}$ and therefore raises the private

innovation component $\lambda_c^d u_{c,t}^{\alpha}$. This yields the feedback loop

$$P_{c,t}^S \downarrow \Rightarrow Y_{c,t}^S \uparrow \Rightarrow \dot{z}_{c,t}/z_{c,t} \uparrow \Rightarrow P_{c,t} \downarrow \Rightarrow e_{c,t}(m) \uparrow, \tag{3.52}$$

subject to the market-size and strategic-prize terms in (3.51).

A positive downstream innovation shock, represented by a higher λ_c^d, strengthens this loop. The FOC implies $\partial \ln Y_c^S / \partial \ln \lambda_c^d = 1/(1-\alpha) > 0$. Hence a higher λ_c^d increases semiconductor absorption by downstream firms, raises the domestic market-size component of E_c^S, and increases productivity growth for any given semiconductor price. This is why an AI-type downstream innovation shock amplifies the short-run gains from cheaper domestic semiconductors and can mitigate the long-run losses from a smaller foreign semiconductor market.

3.3.3 General Equilibrium Trade Balance Linkage

The balance-of-payments condition links semiconductor and downstream adjustments. An export control that directly reduces semiconductor exports must be absorbed through changes in semiconductor wages and prices, downstream trade balances, and bond accumulation. Thus the semiconductor and downstream sectors cannot be evaluated independently.

4 Quantitative Analysis

We now take the model to data and study the quantitative implications of the U.S. semiconductor sanction policies, with various alternative specifications. We think of the policy shocks to be unexpected and permanent. We conduct a transition path analysis to account for both short-run and long-run effects. We assume that the world economy grows along balanced growth path prior to the introduction of policies. Short-run effects are defined as the impacts along the transition between the initial and the new balanced growth paths, while long-run effects are defined as the impacts after the economy has converged to the new balanced growth path. For now, to better isolate the mechanisms of the interplay between semiconductors and downstream sector, we assume the downstream knowledge spillover across countries ι_c is 0.[10]

[10] We find that incorporating this feature does not materially alter our quantitative results. For expositional simplicity, we set it to 0.

4.1 Parameterization

We estimate the model parameters in the initial balanced growth path. We source data from standard public datasets (e.g., World Bank) and our constructed micro-level datasets like ORBIS and ORBIS-IP. We use 2020 as the baseline year for the initial BGP calibration, and stay as close as possible if data for 2020 is not available.

The two economies. The model has two countries. Quantitatively, one is China, and the other is is the US-aligned semiconductor bloc, because the technologies, firms, and export-control coalition the model is about are shared across a handful of economies that behave jointly. Which economies those are is settled from the data rather than from a political list.

We rank economies by the number of semiconductor patent *families* they hold from semiconductor patent identified using IPC codes in Orbis. Table B.5 in the appendix shows that eight economies account for 95.5% of all semiconductor families, and the ninth (RU) is an order of magnitude smaller. Besides China and the United States, the six largest economies are all natural U.S. allies: {JP, KR, TW, DE, FR, NL}, the East Asian fabrication powers plus the three European nodes that hold the critical equipment and device positions. In all the following quantitative results, we simply refer to US, but it should be clear that "US" is measured empirically by the sum of the U.S. and its eight allies.

Table 4.1 reports the parameter values, which can be classified into either externally or internally calibrated parameters. Panel A lists externally set parameters. They are standard values used in the literature. We normalize the semiconductor labor to be one in both economies, and set the innovation subsidies to both semiconductor and downstream sectors to zero in the initial BGP.

4.2 Internally Calibrated Parameters

Panel B of Table 4.1 lists internally estimated parameters, their target moments and data sources. They are estimated using simulated methods of moments. Appendix B.4 explains the detailed construction and measurement of the targeted moments, including bond holdings, the semiconductor sector size, the size and trade of downstream sectors, the semiconductor share of downstream innovation input, the BGP growth rate, and the U.S.-China semiconductor gap distribution.

Figure 4.1 shows our calibration results for the semiconductor technology gap distribution. Panel (a) shows the empirical technology gap distribution for empirical m_{it} over the years 2015–2020, right before U.S. semiconductor export sanction policies. The U.S. semiconductor technology gap relative to China was close to 0, as reflected by a probability mass distribution over the U.S.–China

Table 4.1: Parameterization

Parameters	Notation	Value	Targeted Moments	Data Source
Panel A. External Parameterization				
I. Households				
Discount factor	ρ	0.02	real interest rate	FRED
Bond adjustment cost	η	2	assigned	N.A.
Semiconductor labor	$L_c^S, \forall c$	1.0	normalization	N.A.
II. Downstream Goods				
Elasticity of substitution	σ	5	common estimates	N.A.
Innovation subsidy	κ	0	assigned	N.A.
III. Semiconductors				
Elasticity of substitution	σ^S	5	common estimates	N.A.
Innovation cost elasticity	γ	2	common estimates	N.A.
Innovation subsidy	κ^s	0	assigned	N.A.
Panel B. Internal Parameterization				
I. Households				
Bond holdings	$\bar{B}_U$	1.65	US TB, % of GDP	WDI
II. Downstream Goods				
Labor force	$L_c, \forall c, c'$	5	US semi output, % of GDP	SIA
Trade cost	$d_{cc'}, \forall c, c'$	1.05	US domestic expenditure share	BACI
Innovation efficiency	λ_U^d	0.012	US-CN GDP ratio	PWT
Innovation efficiency	λ_C^d	0.006	CN-US GDP per capita ratio	PWT
Semiconductor input share	α	0.2	US semi share of innovation spending	SIA
III. Semiconductors				
Trade cost	$d_{cc'}^s, \forall c, c'$	1.3	US semiconductor world output share	SIA
Productivity gap	λ	1.2	US TFP growth	PWT
Innovation efficiency	λ_U^s	3.0	Figure 4.1: prob. mass for $m \in [-4, 4]$	ORBIS
Innovation efficiency	λ_C^s	3.1	Figure 4.1: prob. mass for $m \in [5, 13]$	ORBIS
Int'l knowledge spillover	ι^S	0.085	Figure 4.1: prob. mass for $m \in [14, \infty)$	ORBIS

Notes: This table summarizes the parameters and the moments that identify their values. US in the data represents the U.S. and its allies, including JP, KR, TW, DE, FR, and NL.

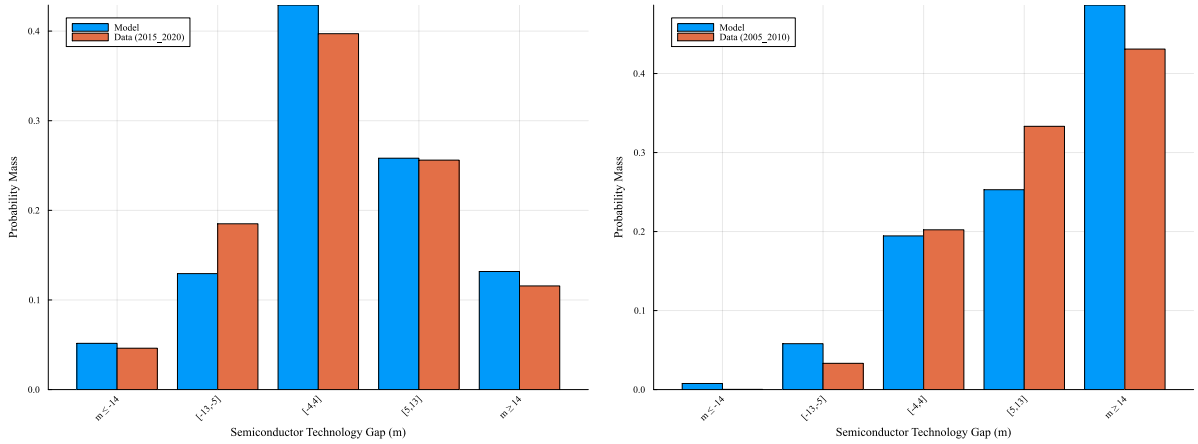
technology gap that is symmetric around 0. The model successfully replicates this pattern. Panel (b) instead shows the parallel model and empirical distribution over the years 2005–2010, which starkly differ from the distribution from ten years later and exhibit a much greater U.S. bloc technology advantage. In one of our alternative counterfactual exercise, we calibrate our model to this distribution and shows how the quantitative implications of semiconductor sanctions are drastically different.

Table 4.2 shows the target-matching results for our baseline calibration.

4.3 Counterfactual Analyses

In this section, we examine the effects of an unexpected and permanent U.S. semiconductor control policy on the transition from the initial balanced growth path (BGP) to a new BGP equilibrium.

Figure 4.1: Semiconductor Technology Gap Distribution: Model VS Data



(a) 2015-2020: grouped

(b) 2005-2010: grouped

Notes: The data in 2015-2020 is used for baseline calibration. The data in 2005-2010 is used for calibration of the counterfactual analysis in section 4.3.5.

Table 4.2: Targeted Moments for Internal Parameterization

Targeted Moment	**Data**	**Model**
US trade balance-GDP ratio	-0.01	-0.01
US semiconductor output share of GDP	0.01	0.02
US domestic expenditure share	0.85	0.73
US-CN GDP ratio	1.58	2.42
CN-US GDP per capita ratio	0.32	0.41
US semiconductor share of innovation spending	0.20	0.20
US semiconductor world output share	0.87	0.71
US TFP growth rate	0.01	0.01
Figure 4.1: prob. mass for $m \in [-4, 4]$	0.40	0.43
Figure 4.1: prob. mass for $m \in [5, 13]$	0.26	0.26
Figure 4.1: prob. mass for $m \in [14, \infty)$	0.12	0.13

Notes: This table summarizes the targeted empirical moments and their corresponding values used for model parameterization. US in the data represents the U.S. and its allies, including JP, KR, TW, DE, FR, and NL.

We introduce a U.S. semiconductor control policy that reduces U.S. exports of high-end semiconductors, as well as high-end semiconductor knowledge spillovers to China, to an infinitesimal level, corresponding to semiconductor control policies in the data.[11] In the model, high-end semi-

[11]The October 2022 U.S. semiconductor controls policy architecture makes this distinction concrete. It not only restricted exports of advanced computing chips, but also imposed licensing requirements on semiconductor-manufacturing equipment and related software and technology, and restricted U.S. persons from supporting advanced-node production at Chinese fabs, including by servicing production equipment. Subsequent rules broadened the covered equipment and design software (U.S. Department of Commerce, Bureau of Industry and Security, 2022, 2023, 2024). Other measures extend beyond export licensing: CHIPS Act guardrails restrict funding recipients from undertaking certain joint research or technology-licensing activities with foreign entities of concern, while the outbound-investment regime prohibits or requires notification of certain investments in Chinese semiconductor activities that may convey managerial assistance, business and talent networks, and market access (U.S. Department

conductors have $m > 0$, i.e., the U.S. has semiconductor technological advantage over China. We find that the transition from the initial BGP to the new BGP takes approximately 620 periods to complete.[12]

4.3.1 Effect of U.S. Semiconductor Control

The transition dynamics reveal a stark divergence between the immediate impact and the long-run equilibrium following the imposition of export controls. Figure 4.2 shows the results.

Semiconductor Growth Panel (a) shows that on impact, U.S. semiconductor growth increases and then gradually declines toward its new BGP level. For approximately the first 200 periods of transition, U.S. semiconductor growth remains higher than its initial BGP level. The mechanisms behind these dynamics are as follows.

On impact, the export control severs U.S. semiconductor producers from Chinese demand. This immediate negative demand shock requires the U.S. semiconductor wage (w^S) to fall in order to clear the domestic semiconductor labor market. Given the markup pricing rule in equation (3.14), this wage reduction translates directly into a lower domestic price for the semiconductor aggregate (P^S). Lower semiconductor prices boost domestic downstream demand, mitigating the negative effect of losing the Chinese market on U.S. semiconductor innovation. On the other hand, reduced knowledge spillovers to China strengthens U.S. semiconductor innovation and growth by increasing their escape-competition motive: U.S. semiconductor firms are more likely to maintain the technology leadership, so they are willing to do more innovation.[13][14]

Over time, these positive growth effects are dominated by the dynamic consequences of diminishing returns of semiconductor innovation. In our endogenous growth framework, innovation

of Commerce, National Institute of Standards and Technology, 2023; U.S. Department of the Treasury, Office of Investment Security, 2024). Taken together, these measures seek not only to constrain China's use of frontier chips, but also to slow the accumulation and diffusion of the capabilities needed to manufacture them.

[12] For now, we interpret 620 periods as 620 years. Later, we will use the event study in the data to discipline the model's short-run responses, which will clarify whether 620 periods correspond to 620 years or fewer.

[13] See Sui (2023) for proof that reducing knowledge spillovers increases the escape-competition motive in a step-by-step innovation framework.

[14] Crucially, the short-run U.S. semiconductor boom is not assumed to follow mechanically from the export ban. Equation (3.51) shows that U.S. semiconductor innovation rises only when the combined domestic market-size response, R&D-cost response, and escape-competition response dominate the lost Chinese market. (i) A lower U.S. semiconductor wage can reduce P_U^S and raise domestic downstream semiconductor absorption, but this channel is quantitatively relevant only if domestic semiconductor expenditure rises enough to offset lost export revenue. (ii) Even when this market-size condition fails, U.S. semiconductor innovation can still rise in the short run if the reduction in knowledge spillovers to China raises the strategic prize $\Delta v_U^S(m)$ sufficiently. (iii) A faster semiconductor growth could help decrease semiconductor price at a faster speed, which benefits downstream innovation and ultimately reduces the semiconductor innovation cost.

investments are determined by not only the scale of semiconductor market size but also the technology gaps between firms. By restricting exports, U.S. firms permanently lose a significant fraction of their global market scale. This depresses expected future profits and reduces the semiconductor innovation incentives ($e_{U,t}(m)$). On the other hand, as the U.S. firms increases the semiconductor technological advantage over China due to their faster growth, they face diminishing escape-competition motives. This contributes to a long-run growth loss.

Panel (a) shows that for China, on impact, semiconductor growth increases and then gradually declines toward its new BGP level. For approximately the first 100 periods of transition, Chinese semiconductor growth remains higher than its initial BGP level. The mechanisms behind these dynamics are as follows.

On impact, several forces are in operation. (i) U.S. export controls cause the U.S. semiconductor market share in China to be lost to Chinese semiconductor producers, which directly increases Chinese producers market share, profits, and hence innovation incentives, all else equal. (ii) The sudden loss of U.S. semiconductor imports forces Chinese downstream firms to substitute toward domestic intermediates, which are less productive and more expensive than U.S. intermediates. To clear the domestic semiconductor labor market and increase demand for Chinese semiconductors, the Chinese semiconductor wage rate falls. Given the lower U.S. semiconductor wage, this wage reduction could mitigate the negative effect on Chinese downstream demand for semiconductors arising from the lower-quality semiconductors supplied by Chinese producers. (iii) Cut off from the technological frontier, the loss of U.S. knowledge diffusion drastically raises the effective cost of innovation for Chinese semiconductor producers. Deprived of these critical spillovers, Chinese innovation incentives are severely dampened. To summarize, Chinese semiconductor growth increases or decreases after export control depends on the relative strength of several different forces. Panel (a) of Figure 4.2 shows that Chinese semiconductor growth increases on impact because the import substitution effect and wage reduction effect are strong. However, over the transition path, the semiconductor growth decreases in China: the negative effect of U.S. knowledge spillover reduction materializes, which slows down Chinese semiconductor growth; slower productivity growth prevents semiconductor prices from declining at their historical rates, persistently dampening semiconductor output growth during the transition and causing China to permanently fall behind in the semiconductor technology race.

Downstream Growth Panel (d) of Figure 4.2 shows that for the U.S., downstream growth increases on impact. For approximately the first 350 periods of transition, downstream growth remains persistently higher than the initial BGP level. Thereafter, downstream growth decreases toward its new BGP level. The mechanisms behind these dynamics are as follows.

On impact, U.S. downstream growth is boosted both by lower semiconductor prices and by the expected higher value of downstream innovation resulting from faster semiconductor growth. Over time, U.S. downstream growth initially rises before declining toward its new BGP level. The initial increase occurs because faster semiconductor growth accelerates price reductions, which incentivizes downstream innovation. The subsequent decline is driven by the diminishing marginal benefit of increasing downstream productivity over time, as a slowdown in semiconductor innovation leads to a slower reduction in semiconductor prices. In the long run, as semiconductor innovation stagnates, semiconductor prices fail to decline at historical rates. Deprived of increasingly cheaper inputs, downstream firms face permanently lower returns on innovation, causing downstream growth to fall below the baseline.

Panel (d) shows that on impact, Chinese downstream growth decreases due to restricted access to advanced U.S. semiconductors needed for downstream innovation. Over time, Chinese downstream growth gradually rises before declining toward its new BGP level. The gradual rise stems from faster domestic semiconductor growth, whereas the subsequent decline is driven by its eventual deceleration.

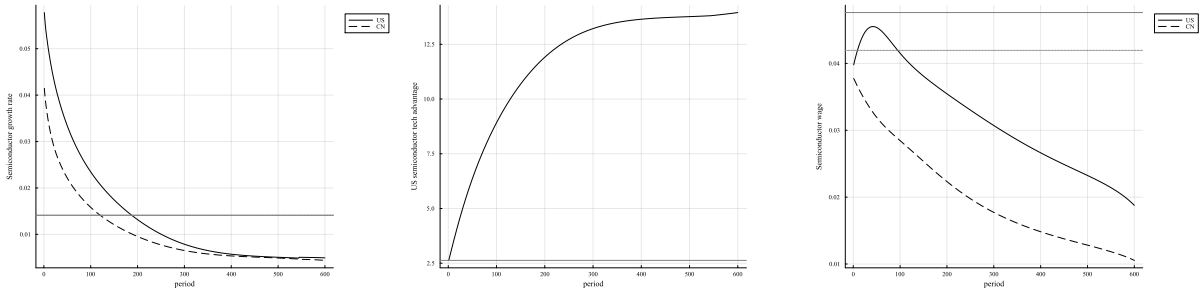
Driven by faster downstream growth in the U.S. relative to China, the U.S. expands its technological lead in the downstream sector. In the long run, although the U.S. widens its technological advantage over China across both sectors, aggregate growth in both sectors slows. This deceleration results from the diminishing escape-competition motive for U.S. semiconductor innovation, a smaller market size for U.S. semiconductor producers, and a discouragement effect on Chinese semiconductor innovation.

4.3.2 Decomposing the Effects of U.S. Semiconductor Control

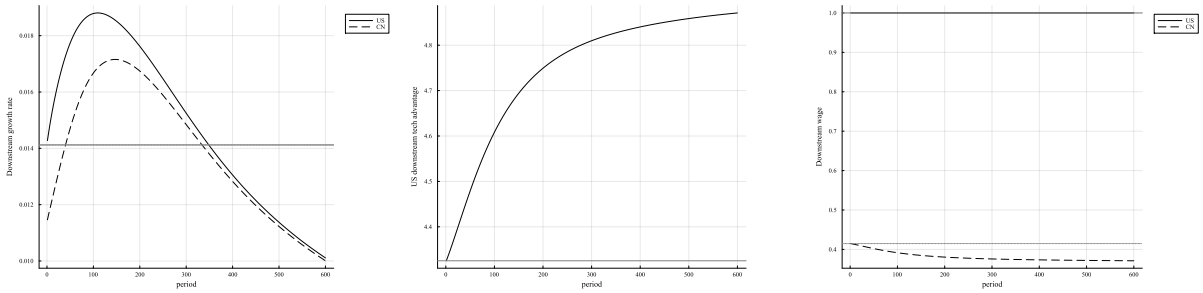
In the baseline analysis above, the effects of U.S. semiconductor controls are driven by two distinct channels: a reduction in U.S. semiconductor exports to China and a reduction in U.S. semiconductor knowledge diffusion to China. In this section, we decompose these effects by modeling a counterfactual scenario where U.S. export controls restrict semiconductor knowledge diffusion to China but keep exporting semiconductors to China. Figure 4.3 shows the results.

Semiconductor Growth Panel (a) shows that, consistent with the baseline, U.S. semiconductor growth increases on impact and then gradually declines toward the new BGP level. This pattern is driven initially by the escape-competition motive and subsequently by its attenuation as the U.S. widens its semiconductor technological advantage over China. Unlike in the baseline case, if the U.S. continues semiconductor exports to China while restricting only knowledge spillovers,

Figure 4.2: Effects of U.S. Semiconductor Control



(a) g^S (b) S Tech Advantage$_{US}$ (c) w^S



(d) g (e) D Tech Advantage$_{US}$ (f) w

Notes: The black solid line shows the transition from the initial BGP to the new BGP for the U.S., while the black dashed line shows the corresponding transition for China. The solid (dotted) horizontal line indicates the initial BGP value in the U.S. (China).

U.S. firms do not suffer from losing the Chinese market; consequently, semiconductor growth on impact is higher than in the baseline. Over time, however, this growth boost dissipates more rapidly than in the baseline due to stronger diminishing returns to escaping competition. Thus, relative to the baseline, the U.S. expands its technological lead over China faster initially, but holds a smaller technological advantage in the long run. Additionally, in this counterfactual scenario, the U.S. semiconductor wage w^S falls less sharply to clear the labor market than in the baseline. Nevertheless, w^S still declines because restricting spillovers lowers Chinese firms' expected returns on innovation (as they are less able to close the technology gap with the U.S.), which ultimately depresses downstream demand for semiconductors.

Panel (a) shows that for China, consistent with the baseline, semiconductor growth increases on impact and then gradually declines toward the new BGP level. This pattern is initially driven by the escape-competition motive and subsequently by the discouragement effect as the U.S. widens its semiconductor technological advantage over China. However, Chinese semiconductor growth remains lower than in the baseline because reduced knowledge spillovers constrain China's growth.

Downstream Growth Panel (d) of Figure 4.3 shows that for the U.S., consistent with the baseline, downstream growth initially increases before declining toward its new BGP level. Unlike in the baseline, however, these dynamics unfold across three phases: during roughly the first 100 transition periods, the surge in downstream growth is less pronounced; between approximately periods 100 and 300, the growth boost is more pronounced; and beyond period 300, the drop in downstream growth is steeper. The reasons are as follows. In the first 100 periods, the initial downstream expansion is weaker because semiconductor wage (and price) reductions are smaller than in the baseline, providing less stimulus to downstream innovation. Between periods 100 and 300, downstream growth becomes stronger because semiconductor price reductions become larger relative to the baseline.[15] Beyond period 300, downstream growth declines more sharply because semiconductor growth decelerates at a faster pace than in the baseline.

Panel (d) shows that for China, downstream growth is faster on impact compared to the baseline because China retains access to advanced U.S. semiconductors for downstream innovation under this counterfactual. Later in the transition, however, downstream growth falls below the baseline due to slower domestic semiconductor growth. Because Chinese downstream growth is faster than in the baseline, the U.S. maintains a smaller downstream technological advantage over China.

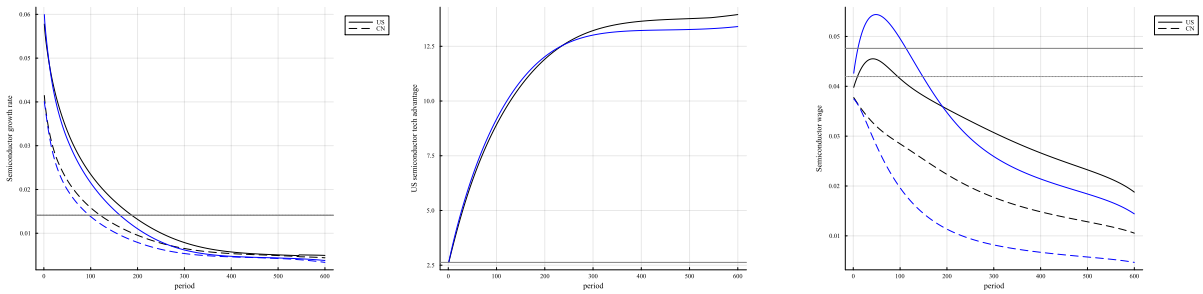
4.3.3 If China Increases Semiconductor Innovation Efficiency

In the baseline analysis in Section 4.3.1, we assume Chinese semiconductor innovation cost ($\lambda_C^s(1-\kappa_C^s)$) is invariant to the export control policy. In this section, we study the effects of U.S. semiconductor controls when China responds by heavily subsidizing its own semiconductor innovation to reach the innovation efficiency level in the U.S. (i.e., $\lambda_U^s(1-\kappa_U^s) = \lambda_C^s(1-\kappa_C^s)$ and $\kappa_U^s = 0$). By introducing semiconductor innovation subsidies, China lowers the effective cost of innovation for its semiconductor firms. Alternatively, this innovation subsidy can be interpreted as any forces that lead to higher semiconductor innovation efficiency in China (e.g., Chinese producers' innovation improvement).

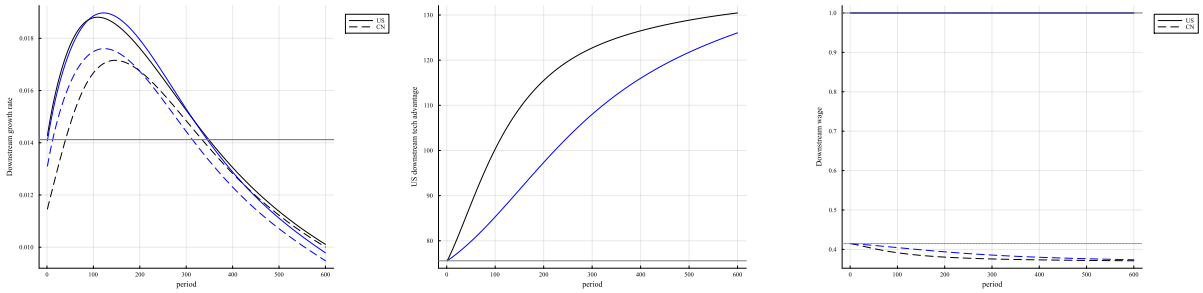
Figure 4.4 displays the results. This Chinese policy response boosts expected returns on innovation in both sectors, mitigating the costs imposed by U.S. knowledge spillover restrictions. Consequently, relative to the baseline, the U.S. holds a smaller technological advantage over China across both sectors. However, the growth difference compared to the baseline is minimal because, along the initial BGP, the U.S. and China have very similar semiconductor innovation efficiencies

[15] From this phase onward, the semiconductor wage declines relative to the baseline because restricting spillovers lowers Chinese firms' expected returns on innovation (as they are less able to close the technology gap with the U.S.) and U.S. semiconductor innovation faces faster diminishing returns, which ultimately depresses downstream demand for semiconductors.

Figure 4.3: Only Semiconductor Technology Spillover Reduction



(a) g^S (b) S Tech Advantage$_{US}$ (c) w^S



(d) g (e) D Tech Advantage$_{US}$ (f) w

Notes: The blue lines represent the values in this counterfactual economy. The remaining lines represent the effects of U.S. semiconductor controls discussed in Figure 4.2 of Section 4.3.1.

($\lambda_U^s = 3.0$ and $\lambda_C^s = 3.1$).

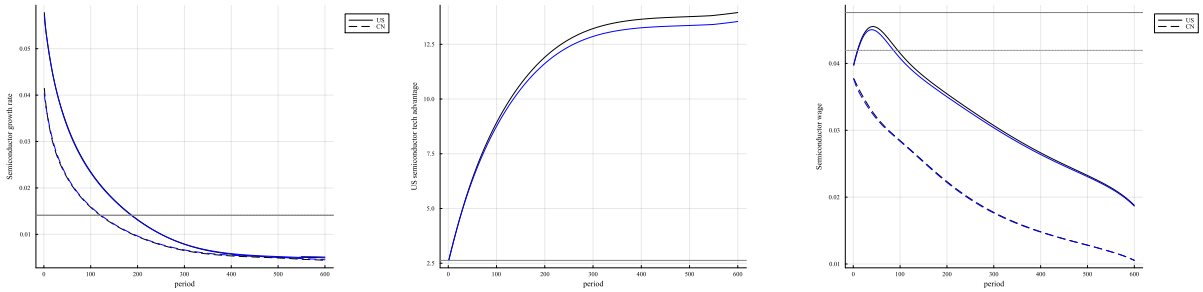
4.3.4 Positive Downstream Innovation Shock

Figure 4.5 shows the effects of a positive downstream innovation shock to both countries (black lines) as well as the effects of U.S. semiconductor controls in the presence of a positive downstream innovation shock to both countries (blue lines). A positive downstream innovation shock is captured by an increase in downstream innovation efficiency (λ_c) by 5 percent in both countries. The transition finishes within 40 periods.

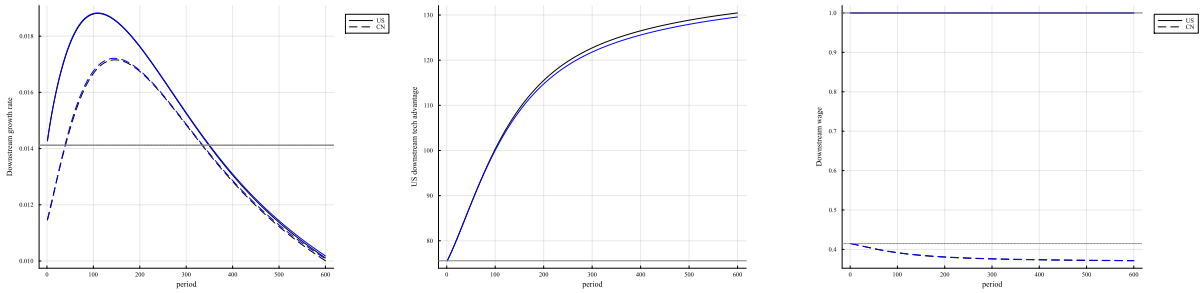
This shock alone (black lines) raises returns to innovation for downstream firms, increasing their demand for semiconductors. To supply more semiconductors to downstream sectors, the semiconductor wage declines relative to the baseline. Consequently, this shock accelerates growth in both the semiconductor and downstream sectors.

Comparing the blue and black lines in Figure 4.5 shows that U.S. semiconductor controls, in the presence of a downstream innovation shock, generate patterns similar to the baseline case shown in Figure 4.2.

Figure 4.4: If China Increases Semiconductor Innovation Efficiency



(a) g^S (b) S Tech Advantage$_{US}$ (c) w^S



(d) g (e) D Tech Advantage$_{US}$ (f) w

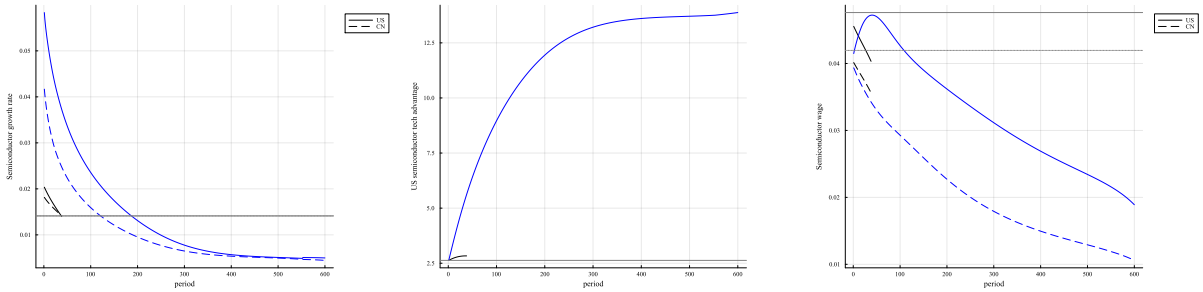
Notes: The blue lines represent the values in this counterfactual economy. The remaining lines represent the effects of U.S. semiconductor controls discussed in Figure 4.2 of Section 4.3.1.

Comparing the blue lines in Figure 4.5 with the baseline curves in Figure 4.2 shows that when U.S. export controls redirect semiconductors domestically at lower prices, the presence of a downstream innovation shock acts as a demand multiplier. This multiplier amplifies the initial transition boom, producing larger initial spikes in semiconductor growth (g^S) and downstream growth (g) relative to the baseline effects of export controls. Moreover, this shock mitigates U.S. semiconductor revenue losses in the Chinese market, leading to faster growth in semiconductor innovation. For China, the positive downstream innovation shock likewise generates a massive surge in demand for semiconductor inputs from downstream firms. Under U.S. export controls, this booming demand cannot be met by advanced U.S. imports and is entirely channeled to domestic Chinese semiconductor producers. This captive and rapidly expanding market creates a powerful "semiconductor market size effect" for Chinese firms, boosting their expected returns on innovation and partially offsetting the costs of lost U.S. knowledge spillovers.

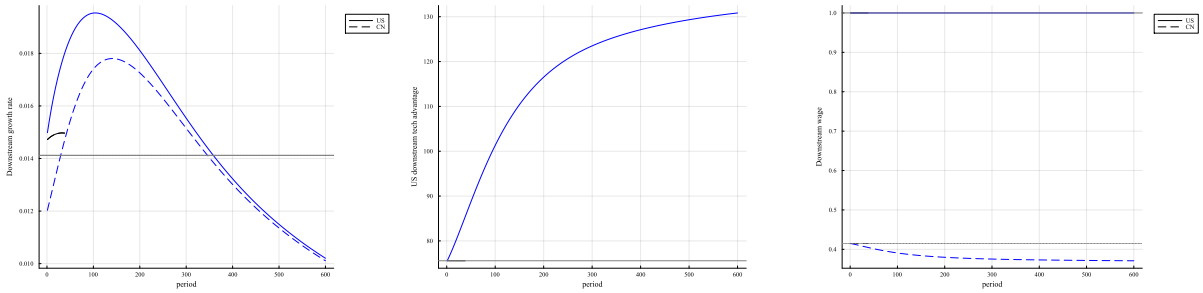
4.3.5 If the Initial U.S. Semiconductor Technology Advantage is High

In this section, we conduct an alternative parameterization to highlight how the effects of U.S. semiconductor control depend on the initial semiconductor technological advantage of the U.S.

Figure 4.5: If Positive Downstream Innovation Shock



(a) g^S (b) S Tech Advantage$_{US}$ (c) w^S



(d) g (e) D Tech Advantage$_{US}$ (f) w

Notes: The black lines represent the effects of downstream innovation shock. The blue lines represent the effects of downstream innovation shock and U.S. semiconductor control. The solid (dotted) horizontal line indicates the initial BGP value in the U.S. (China).

Compared to the baseline parameterization, we increase the U.S. semiconductor innovation efficiency by reducing λ_U^s to 2.3 to generate higher initial U.S. semiconductor technology advantage, mimicking the data pattern from 2005 to 2010. Figure 4.1 shows that during the years 2005–2010, the U.S. semiconductor technology gap relative to China was high, as reflected by a probability mass distribution over the U.S.–China technology gap that is concentrated at technology gaps significantly above 0; the reestimated model successfully replicates this pattern.

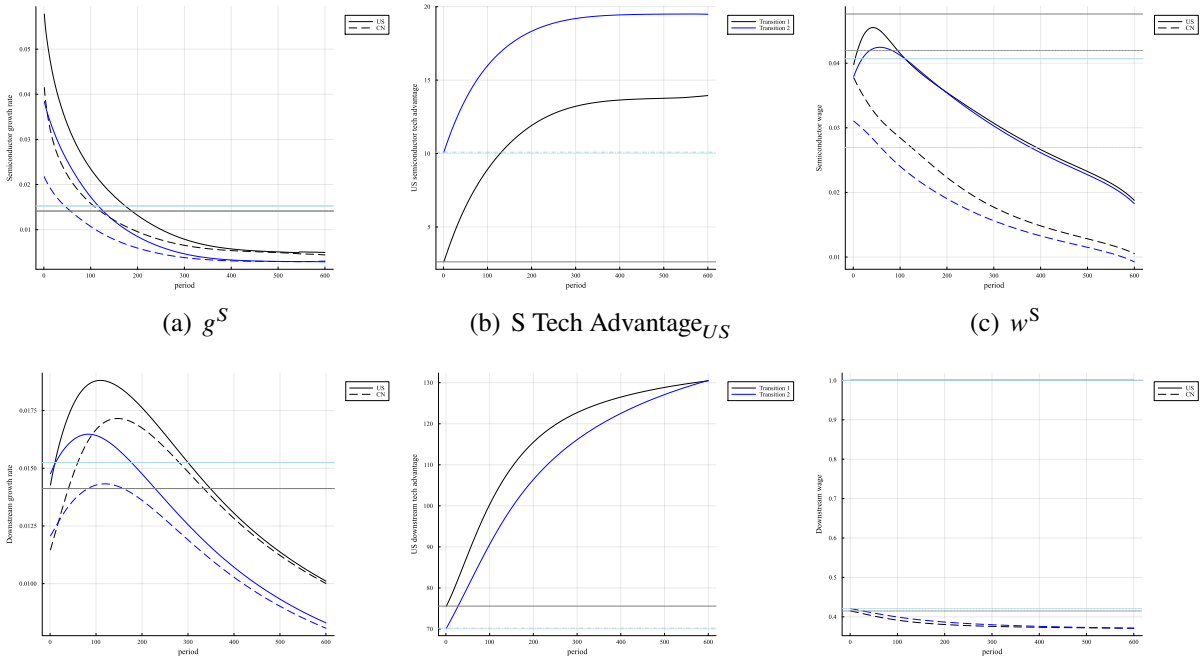
We then introduce an export control policy starting from this initial BGP. Figure 4.6 illustrates the quantitative results. We find that the short-run positive growth effect on the semiconductor sector is smaller for both countries, while the short-run positive growth effect on the downstream sector is smaller in the U.S. and disappears entirely in China. Furthermore, the long-run growth effect is still negative, even though the U.S. increases its technological advantage over China across both sectors.

In the step-by-step innovation framework, a firm's incentive to innovate is heavily driven by the "escape-competition" motive. If the U.S. already possesses a massive technological lead, this motive is largely exhausted. Furthermore, an overwhelming U.S. lead implies that U.S. firms were already capturing maximum global market share. Severing access to the Chinese market under these

conditions imposes a severe loss of expected global profits. The domestic substitution effect via semiconductor wage reductions is insufficient to offset this massive revenue loss. Consequently, the short-run positive growth boom for U.S. semiconductors is severely attenuated. This highlights that export controls are highly unfavorable if the imposing country has already "won" the technology race.

As for China, due to the substantial U.S. lead in semiconductors, Chinese semiconductor growth along the initial BGP relies heavily on knowledge spillovers from the U.S. Thus, U.S. export controls generate a much weaker escape-competition motive for China, as Chinese firms are increasingly discouraged as the U.S. technological lead widens. Additionally, downstream growth experiences no short-run boom, as the muted surge in semiconductor growth is insufficient to raise downstream firms' expected returns to innovation.

Figure 4.6: Effects of U.S. Semiconductor Control in 2010



(a) g^S (b) S Tech Advantage$_{US}$ (c) w^S

(d) g (e) D Tech Advantage$_{US}$ (f) w

Notes: The solid lines show the transition from the initial BGP to the new BGP for the U.S., while the dashed lines show the corresponding transition for China. Solid and dotted horizontal lines indicate the initial BGP values for the U.S. and China, respectively. Black lines represent the baseline scenario from Figure 4.2. Blue lines depict a scenario with a lower initial U.S. semiconductor innovation cost, generating a higher initial U.S. technological advantage in semiconductors.

4.3.6 Effects on Welfare

Table 4.3 presents the welfare effects under different scenarios mentioned above. Panel A shows that in the baseline case, U.S. semiconductor controls increase U.S. welfare by 1.08 percent (in consumption-equivalent terms) while decreasing China's welfare by 0.81 percent. The U.S. experiences welfare gains due to a short-run innovation boom in both sectors, though the gains are modest because more resources are devoted to semiconductor innovation investment rather than household consumption. Conversely, China suffers welfare losses driven by the immediate downstream innovation bust following the U.S. policy, as well as the diversion of resources from household consumption to semiconductor innovation investment.

Panel B shows that if the U.S. only reduces semiconductor knowledge spillovers to China while maintaining semiconductor exports, the U.S. achieves larger welfare gains and China incurs smaller welfare losses relative to the baseline. This is mainly because China's immediate downstream growth following the U.S. policy is faster than in the baseline, which benefits U.S. consumption through downstream trade, and because fewer resources are diverted from household consumption to semiconductor innovation investment. Fewer resources are diverted because reduced knowledge spillovers ultimately decrease semiconductor innovation not only in China, but also in the U.S. due to a weakened escape-competition motive.

Panel C shows that if China improves semiconductor innovation efficiency in response to U.S. policy, the U.S. achieves larger welfare gains and China incurs smaller welfare losses relative to the baseline. This is because in this scenario, China is better able to supply more productive semiconductors to domestic downstream sectors compared to the baseline, leading to faster downstream growth. This faster growth not only increases the production of final goods to mitigate China's welfare loss, but also benefits U.S. consumption through downstream trade.

Comparing Panel A and Panel E shows that if U.S. semiconductor controls are implemented and followed by a positive downstream innovation shock worldwide, both the U.S. and China achieve higher welfare. A downstream innovation shock acts as a semiconductor demand multiplier, which mitigates the negative effect on the U.S. from losing the Chinese market and promotes China's semiconductor innovation through increased demand.

Comparing Panel D and Panel E shows that when a positive downstream innovation shock occurs worldwide, the implementation of U.S. semiconductor controls generates a welfare gain for the U.S. but a loss for China. Relative to the baseline in Panel A, U.S. welfare gains are smaller and Chinese welfare losses are larger. For the U.S., this occurs because while the global downstream innovation shock expands the overall semiconductor market, export controls cause the U.S. to forgo substantial profits from selling to China. For China, semiconductors are critically needed as innovation inputs

to materialize the downstream innovation shock, but U.S. policy deprives China of this opportunity.

Panel F shows that if U.S. semiconductor controls are implemented when the U.S. possesses a much larger initial technological advantage over China, both countries incur welfare losses, with China suffering greater losses. The U.S. experiences welfare losses because U.S. semiconductor firms have a weaker escape-competition motive: given the substantial initial U.S. lead, restricting knowledge spillovers renders China even less likely to overtake the U.S. Compared to the baseline, this leads to a smaller short-run semiconductor innovation boom and a larger long-run innovation bust, which depresses downstream innovation and yields a net welfare loss for the U.S. For China, when the initial technological gap is wide, knowledge spillovers are a primary driver of semiconductor growth. Cutting off these spillovers dampens China's growth, which not only diminishes its short-run semiconductor boom but also causes downstream growth to slow sharply or even turn negative in the short run.

Table 4.3: Welfare Effects

Scenario	US	CN
A. Baseline export controls (trade and knowledge-spillover reductions)	1.08	-0.81
B. Export controls: knowledge-spillover reduction only	1.38	-0.11
C. Export controls with improved CN semiconductor innovation efficiency	1.12	-0.62
D. = D2-D1	0.18	-1.66
D1. Downstream AI shock	1.79	1.72
D2. Downstream AI shock and export controls	1.97	0.06
E. Export controls in 2010	-0.67	-1.94

Notes: Entries report consumption-equivalent welfare changes, in percent. Welfare is computed using equation (3.41), with $T \to \infty$.

5 Conclusion

This paper studies the dynamic effects of U.S. semiconductor controls in a two-country endogenous growth framework disciplined by new empirical evidence. Our quantitative analysis highlights a central intertemporal trade-off. U.S. export controls generate a *short-run boom* in U.S. semiconductor and downstream innovation: domestic semiconductor firms face stronger escape-competition incentives, and domestic downstream firms benefit from a temporary increase in local semiconductor supply. At the same time, Chinese downstream innovation is immediately dampened by reduced access to critical innovation inputs, though Chinese semiconductor innovation can be incentivized in response to U.S. semiconductor producers' heightened escape-competition motive.

However, these gains do not persist. In the *long run*, the loss of access to the Chinese market

reduces the scale of returns to U.S. semiconductor innovation, which then weakens innovation incentives in both the semiconductor sector and downstream industries. This long-run mechanism operates even in scenarios where the U.S. maintains or expands its technological lead over China. Hence, widening the technology gap is not sufficient to guarantee stronger long-run domestic innovation performance.

We further show that broader technological conditions matter for policy outcomes. A positive downstream innovation shock, such as rapid AI-related progress, amplifies short-run benefits from export controls in both semiconductor and downstream sectors. This result suggests that the macro-innovation environment can materially change the effectiveness of trade and technology restrictions.

Overall, our findings imply that semiconductor controls should be evaluated as dynamic innovation policies rather than static trade measures. The short-run national innovation gains can coexist with long-run innovation costs, and complementary domestic policies (e.g., R&D support and downstream innovation capacity building) are critical for improving long-run outcomes. Future work can extend the framework to multi-country supply chains, endogenous policy responses by trading partners, and richer policy mixes that jointly target security and growth objectives.

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Online Appendix for "Controlling Critical Innovation Inputs: Semiconductors in U.S.–China Technology Competition" by Haishi Li, Xiaomei Sui, and Sifan Xue

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A Model Appendix

Throughout this appendix, notation follows the baseline model in the main text. Let

$$E_{c,t} \equiv P_{c,t}Y_{c,t}, \qquad E^S_{c,t} \equiv P^S_{c,t}Y^S_{c,t}, \tag{A.1}$$

denote final-good expenditure and semiconductor-aggregate expenditure. Let

$$r^d_t \equiv \frac{z_{U,t}}{z_{C,t}} \tag{A.2}$$

be the downstream technology ratio. The semiconductor step size is the same $\lambda > 1$ used in the main text. For semiconductor type ω,

$$m_t(\omega) = k_{U,t}(\omega) - k_{C,t}(\omega), \qquad \frac{z^S_{U,t}(\omega)}{z^S_{C,t}(\omega)} = \lambda^{m_t(\omega)}. \tag{A.3}$$

The export-control indicator is written as $\chi_{\omega od,t} \equiv 1_{\text{export}_{\omega od,t}}$, where o is the origin and d is the destination.

A.1 Model Derivations and Properties in BGP

A.1.1 Household Problem

The total profits rebated to household are

$$D_{c,t} = \Pi_{c,t} - P^S_{c,t}(1-\kappa_c)Y^S_{c,t} + \sum_m [\Pi^S_{c,t}(m)P^S_{c,t}Y^S_{c,t} - P_{c,t}RD^S_{c,t}(m)]\mu_t(m), \tag{A.4}$$

where $\Pi_{c,t}$ denotes the production profits of downstream firms, and $\sum_m \Pi^S_{c,t}(m)P^S_{c,t}Y^S_{c,t}\mu_t(m)$ denotes the production profits of semiconductor firms. $\mathrm{Tr}_{c,t}$ denotes net lump-sum transfers. The transfer term includes rebated quadratic adjustment costs (entered positively) and government subsidies to domestic firms that are funded by households (entered negatively). $\sum_m P_{c,t}RD^S_{c,t}(m)\mu_t(m)$ denotes semiconductor sector's innovation cost, and $P^S_{c,t}(1-\kappa_c)Y^S_{c,t}$ denotes downstream firms' expenditures on semiconductors. The utility maximization problem leads to a standard Euler equation:

$$\eta(B_{c,t} - \bar{B}_c) + \frac{\dot{P}_{c,t}}{P_{c,t}} + \frac{\dot{C}_{c,t}}{C_{c,t}} + \rho = R_t, \tag{A.5}$$

where $\frac{\dot{C}_{c,t}}{C_{c,t}}$ and $\frac{\dot{P}_{c,t}}{P_{c,t}}$ denote the growth rate of consumption and final good price.[16]

A.1.2 Downstream Firms' Static Production Decisions

Given the production technology, the labor required to produce $y_{c,t}$ is $l_{c,t} = y_{c,t}z_{c,t}^{-\frac{1}{\sigma-1}}$. Cost minimization implies a constant marginal cost of production $MC_{c,t} = w_{c,t}z_{c,t}^{-\frac{1}{\sigma-1}}$.

Downstream firms engage in monopolistic competition. Their profit maximization problem yields a constant markup over marginal cost:

$$p_{c,t} = \frac{\sigma}{\sigma-1}\frac{w_{c,t}}{z_{c,t}^{\frac{1}{\sigma-1}}}. \tag{A.6}$$

We denote the profits of downstream firms selling from country c to c' by $\pi_{cc',t}$ and their market share in c' by $s_{cc',t}$.

The optimal profit of the downstream producer is the sum of profits across all destination

[16] Throughout the paper, R_t denotes the instantaneous net interest rate paid on the bond stock held at time t. In discrete transition computations, R_n denotes the interest rate over the interval $[t_n, t_{n+1})$. Therefore the discount factor from t_n to t_{n+1} uses $\exp(-R_n\Delta t)$, and bond accumulation over the same interval uses $R_nB_{c,n}$.

markets,

$$\Pi_{c,t} = \sum_{c' \in \mathbb{C}} \pi_{cc',t}, \tag{A.7}$$

where the profit from selling to country c' is given by

$$\pi_{cc',t} = (p_{c,t} - MC_{c,t}) d_{cc'} y_{cc',t} = \frac{1}{\sigma} p_{c,t} d_{cc'} y_{cc',t} = \frac{1}{\sigma} s_{cc',t} P_{c',t} Y_{c',t}, \tag{A.8}$$

and the market share of the producer from country c in country c' is defined as

$$s_{cc',t} = \left(\frac{d_{cc'} p_{c,t}}{P_{c',t}} \right)^{1-\sigma} = \frac{\left(d_{cc'} \frac{\sigma}{\sigma-1} w_{c,t} z_{c,t}^{-\frac{1}{\sigma-1}} \right)^{1-\sigma}}{\sum_{k \in \mathbb{C}} \left(d_{kc'} \frac{\sigma}{\sigma-1} w_{k,t} z_{k,t}^{-\frac{1}{\sigma-1}} \right)^{1-\sigma}} = \frac{1}{\sum_{k \in \mathbb{C}} \left(\frac{d_{kc'} w_{k,t}}{d_{cc'} w_{c,t}} \right)^{1-\sigma} \frac{z_{k,t}}{z_{c,t}}}. \tag{A.9}$$

Accordingly, the final good price can be rewritten as

$$P_{c,t} = \left(d_{cc} \frac{\sigma}{\sigma - 1} \frac{w_{c,t}}{z_{c,t}^{\frac{1}{\sigma-1}}} \right) \left[1 + \sum_{k \neq c} \left(\frac{d_{kc} w_{k,t}}{d_{cc} w_{c,t}} \right)^{1-\sigma} \frac{z_{k,t}}{z_{c,t}} \right]^{\frac{1}{1-\sigma}}. \tag{A.10}$$

Therefore, the total exports of the downstream firm from country c to country c' are

$$\mathrm{EX}_{cc',t} = d_{cc'} p_{c,t} y_{cc',t} = s_{cc',t} P_{c',t} Y_{c',t}. \tag{A.11}$$

A.1.3 Semiconductor Firm's Static Production Decisions

Given a semiconductor firm's pricing rule (3.14), its market share in the market c' equals

$$s^S_{cc',t}(\omega) \equiv \frac{1^{\text{export}}_{c'c}(\omega) d^S_{cc'} p^S_{cc',t}(\omega) y^S_{cc',t}(\omega)}{\sum_{c \in \mathbb{C}} 1^{\text{export}}_{c'c}(\omega) d^S_{cc'} p^S_{cc',t}(\omega) y^S_{cc',t}(\omega)} = 1^{\text{export}}_{c'c}(\omega) \left(\frac{d^S_{cc'} p^S_{cc',t}(\omega)}{P^S_{c',t}(\omega)} \right)^{1-\sigma^S}, \tag{A.12}$$

$P^S_{c,t}$ denotes the aggregate semiconductor price satisfying

$$P^S_{c,t} = \exp\left(\int_0^1 \ln \left[P^S_{c,t}(\omega) \right] d\omega \right). \tag{A.13}$$

The production profit of an intermediate semiconductor producer in country c supplying variety

ω to country $c' \in \mathbb{C}$ is given by

$$\pi^S_{cc',t}(\omega) = [(1 - \frac{\varepsilon_{cc',t}(\omega) - 1}{\varepsilon_{cc',t}(\omega)}) s^S_{cc',t}(\omega)] P^S_{c',t} Y^S_{c',t}, \tag{A.14}$$

so the total production profit of this semiconductor intermediate producer is $\Pi^S_{c,t}(\omega) P^S_{c,t} Y^S_{c,t}$, where

$$\Pi^S_{c,t}(\omega) = \frac{\sum_{c' \in \mathbb{C}} \pi^S_{cc',t}(\omega)}{P^S_{c,t} Y^S_{c,t}} = [(1 - \frac{\varepsilon_{cc,t}(\omega) - 1}{\varepsilon_{cc,t}(\omega)}) s^S_{cc,t}(\omega)] + [(1 - \frac{\varepsilon_{cc',t}(\omega) - 1}{\varepsilon_{cc',t}(\omega)}) s^S_{cc',t}(\omega)] \frac{P^S_{c',t} Y^S_{c',t}}{P^S_{c,t} Y^S_{c,t}}. \tag{A.15}$$

Alternatively, total semiconductor operating profits can be written as

$$\sum_{c' \in \mathbb{C}} \pi^S_{cc',t}(\omega) = \Pi^S_{c,t}(\omega) P^S_{c,t} Y^S_{c,t}, \qquad \Pi^S_{c,t}(\omega) = \sum_{c' \in \mathbb{C}} \frac{s^S_{cc',t}(\omega)}{\varepsilon_{cc',t}(\omega)} \frac{P^S_{c',t} Y^S_{c',t}}{P^S_{c,t} Y^S_{c,t}}. \tag{A.16}$$

Equation (A.16) is the object that enters the semiconductor producer's HJB: it shows explicitly that semiconductor profits are determined by technology-gap-dependent market shares and markups, destination semiconductor expenditures, and market access.

A.1.4 Productivity-Level Normalization and Absolute-Level Recovery

The baseline model is formulated in absolute productivity levels. A stationary BGP computation, however, can only determine levels relative to a technology unit. The natural unit is the world semiconductor frontier. For each semiconductor variety ω, define

$$K^F_t(\omega) \equiv \max\{k_{U,t}(\omega), k_{C,t}(\omega)\}, \qquad a^F_t(\omega) \equiv \lambda^{K^F_t(\omega)}. \tag{A.17}$$

The aggregate world semiconductor frontier level is the geometric mean

$$A^F_t \equiv \exp\left(\int_0^1 \log a^F_t(\omega) d\omega \right). \tag{A.18}$$

For a variety with gap $m = k_U - k_C$, the country-specific semiconductor productivities are

$$z^S_{U,t}(\omega) = a^F_t(\omega) \lambda^{\min\{m,0\}}, \tag{A.19}$$

$$z^S_{C,t}(\omega) = a^F_t(\omega) \lambda^{-\max\{m,0\}}. \tag{A.20}$$

Therefore define the frontier-normalized variety productivities

$$\widehat{z}_U^S(m) \equiv \lambda^{\min\{m,0\}}, \qquad \widehat{z}_C^S(m) \equiv \lambda^{-\max\{m,0\}}. \tag{A.21}$$

The aggregate country-level semiconductor productivity indices are

$$A_{U,t}^S \equiv \exp\left(\int_0^1 \log z_{U,t}^S(\omega) d\omega\right) = A_t^F \lambda^{\sum_{m<0} m\mu_t(m)}, \tag{A.22}$$

$$A_{C,t}^S \equiv \exp\left(\int_0^1 \log z_{C,t}^S(\omega) d\omega\right) = A_t^F \lambda^{-\sum_{m>0} m\mu_t(m)}. \tag{A.23}$$

Hence

$$\frac{A_{U,t}^S}{A_{C,t}^S} = \lambda^{\sum_m m\mu_t(m)}, \qquad \sum_m m\mu_t(m) = \frac{\log A_{U,t}^S - \log A_{C,t}^S}{\log \lambda}. \tag{A.24}$$

The aggregate frontier level A_t^F is not pinned down by stationary BGP equations. It is a normalization. In the initial BGP, the policy-date normalization is

$$A_0^{F,\text{old}} = 1, \qquad A_t^{F,\text{old}} = \exp(g^{S,\text{old}} t). \tag{A.25}$$

Thus, at $t = 0$, initial raw levels equal initial relative levels. The new BGP can be solved as a stand-alone stationary system using $\check{A}_0^{F,\text{new}} = 1$, but this normalization is only a computational device. When the new BGP is connected to a transition ending at T, its absolute frontier is

$$A_t^{F,\text{new}|T} = A_T^F \exp\left(g^{S,\text{new}}(t-T)\right), \qquad t \geq T, \tag{A.26}$$

where

$$A_T^F = \exp\left(\int_0^T g_s^S ds\right) \quad \text{or, on the numerical grid,} \quad A_N^F = \exp\left(\sum_{n=0}^{N-1} g_n^S \Delta t\right). \tag{A.27}$$

Therefore the transition-connected new BGP generally has

$$A_T^{F,\text{new}|T} = A_T^F \neq 1. \tag{A.28}$$

For downstream productivity, define

$$\widehat{z}_{c,t} \equiv \frac{z_{c,t}}{A_t^F}, \qquad z_{c,t} = A_t^F \widehat{z}_{c,t}. \tag{A.29}$$

The numerical BGP object called the downstream productivity level is $\widehat{z}_c$, not the raw level $z_{c,t}$. In the initial BGP,

$$z_{c,t}^{\text{old}} = A_t^{F,\text{old}} \widehat{z}_c^{\text{old}} = \exp(g^{S,\text{old}} t) \widehat{z}_c^{\text{old}}. \tag{A.30}$$

In the transition-connected new BGP,

$$z_{c,t}^{\text{new}|T} = A_t^{F,\text{new}|T} \widehat{z}_c^{\text{new}} = A_T^F \exp\left(g^{S,\text{new}}(t-T)\right) \widehat{z}_c^{\text{new}}. \tag{A.31}$$

Along the transition,

$$A_{n+1}^F = A_n^F \exp(g_n^S \Delta t), \qquad z_{c,n} = A_n^F \widehat{z}_{c,n}. \tag{A.32}$$

Final-good and semiconductor prices are stationarized by

$$\widehat{P}_{c,t}^S \equiv A_t^F P_{c,t}^S, \qquad \widehat{P}_{c,t} \equiv (A_t^F)^{1/(\sigma-1)} P_{c,t}. \tag{A.33}$$

The semiconductor innovation shifter is

$$Q_{c,t}^S \equiv (A_t^F)^{1/(\sigma-1)}, \qquad P_{c,t} Q_{c,t}^S = \widehat{P}_{c,t}. \tag{A.34}$$

Consequently, all stationary BGP equations are expressed in hatted objects. Raw productivity and raw quantities are recovered only after multiplying by the appropriate frontier level A_t^F.

The semiconductor price in country c at period t can be rewritten as

$$\ln(P_{c,t}^S) = \sum_m \ln(P_{c,t}^s(m)) \mu_t(m) = -\ln(A_{c,t}^S) + CON_{c,t}, \tag{A.35}$$

where

$$CON_{c,t} = \frac{1}{1-\sigma^S} \sum_m \ln \left[\left(\frac{\varepsilon_{cc,t}(m)}{\varepsilon_{cc,t}(m) - 1} w_{c,t}^S \right)^{1-\sigma^S} + 1_{\text{export}_{\omega c' c}} \left(d_{c'c}^S \frac{\varepsilon_{c'c,t}(m)}{\varepsilon_{c'c,t}(m) - 1} w_{c',t}^S \right)^{1-\sigma^S} \left(\frac{z_{c',t}^S(m)}{z_{c,t}^S(m)} \right)^{\sigma^S - 1} \right] \mu_t(m) \tag{A.36}$$

Along a BGP, relative semiconductor productivities, market-access indicators, market shares, markups, and semiconductor wages are stationary, so $CON_{d,t}^S$ is constant and $g_{P_d^S} = -g^S$.

A.1.5 Derivation of the Semiconductor Price Normalization

This subsection derives why the downstream-productivity normalization

$$\widehat{z}_{c,t} \equiv \frac{z_{c,t}}{A_t^F} \tag{A.37}$$

is paired with the semiconductor-price normalization

$$\widehat{P}^S_{c,t} \equiv A_t^F P^S_{c,t}. \tag{A.38}$$

Here A_t^F denotes the world semiconductor technology frontier. The key point is that (A.38) is not an independent assumption. It follows from the fact that semiconductor productivity grows in proportion to A_t^F, so semiconductor unit costs and semiconductor prices fall in proportion to $1/A_t^F$.

Step 1: Normalize downstream productivity by the semiconductor frontier. The numerical BGP object is the downstream productivity level relative to the world semiconductor frontier:

$$\widehat{z}_{c,t} = \frac{z_{c,t}}{A_t^F}. \tag{A.39}$$

Equivalently,

$$z_{c,t} = A_t^F \widehat{z}_{c,t}. \tag{A.40}$$

On a BGP, $\widehat{z}_{c,t}$ is stationary, while the raw downstream productivity level $z_{c,t}$ grows at the same rate as the semiconductor frontier:

$$\frac{\dot{z}_{c,t}}{z_{c,t}} = \frac{\dot{A}_t^F}{A_t^F} = g^S. \tag{A.41}$$

Step 2: Normalize semiconductor intermediate productivity by the same frontier. For a semiconductor intermediate with technology gap m, write country-o's semiconductor productivity as

$$z^S_{o,t}(m) = A_t^F \widehat{z}^S_o(m), \tag{A.42}$$

where $\widehat{z}_o^S(m)$ is the semiconductor productivity of country o relative to the world frontier. For example, under the gap convention $m = k_U - k_C$,

$$\widehat{z}_U^S(m) = \lambda^{\min\{m,0\}}, \qquad \widehat{z}_C^S(m) = \lambda^{-\max\{m,0\}}. \tag{A.43}$$

Thus a country at the frontier has relative productivity equal to one, while a laggard is below the frontier by the relevant number of rungs.

Step 3: Semiconductor marginal costs scale as $1/A_t^F$. The semiconductor production technology is

$$y_{o,t}^S(m) = z_{o,t}^S(m) l_{o,t}^S(m). \tag{A.44}$$

Therefore the unit labor requirement is $1/z_{o,t}^S(m)$, and the marginal cost of producing semiconductor intermediate m in country o is

$$MC_{o,t}^S(m) = \frac{w_{o,t}^S}{z_{o,t}^S(m)}. \tag{A.45}$$

Using (A.42),

$$MC_{o,t}^S(m) = \frac{w_{o,t}^S}{A_t^F \widehat{z}_o^S(m)} = \frac{1}{A_t^F} \frac{w_{o,t}^S}{\widehat{z}_o^S(m)}. \tag{A.46}$$

Hence, holding the stationary semiconductor wage $w_{o,t}^S$ fixed, semiconductor marginal costs fall one-for-one with the world semiconductor frontier.

Step 4: Semiconductor intermediate prices also scale as $1/A_t^F$. The semiconductor pricing rule is

$$p_{od,t}^S(m) = \frac{\varepsilon_{od,t}^S(m)}{\varepsilon_{od,t}^S(m) - 1} \frac{w_{o,t}^S}{z_{o,t}^S(m)}. \tag{A.47}$$

Substituting $z^S_{o,t}(m) = A^F_t \widehat{z}^S_o(m)$, we get

$$p^S_{od,t}(m) = \frac{\varepsilon^S_{od,t}(m)}{\varepsilon^S_{od,t}(m) - 1} \frac{w^S_{o,t}}{A^F_t \widehat{z}^S_o(m)}$$
$$= \frac{1}{A^F_t} \underbrace{\left[\frac{\varepsilon^S_{od,t}(m)}{\varepsilon^S_{od,t}(m) - 1} \frac{w^S_{o,t}}{\widehat{z}^S_o(m)} \right]}_{\equiv \widehat{p}^S_{od,t}(m)}. \tag{A.48}$$

Therefore,

$$p^S_{od,t}(m) = \frac{\widehat{p}^S_{od,t}(m)}{A^F_t}, \qquad \widehat{p}^S_{od,t}(m) = A^F_t \, p^S_{od,t}(m). \tag{A.49}$$

Step 5: The semiconductor CES price index inherits the same normalization. For destination country d, the semiconductor variety-m price index is

$$P^S_{d,t}(m) = \left[\sum_{o \in C} \chi_{od,t}(m) \left(d^S_{od} p^S_{od,t}(m) \right)^{1-\sigma^S} \right]^{\frac{1}{1-\sigma^S}}, \tag{A.50}$$

where $\chi_{od,t}(m)$ is the market-access indicator. Using $p^S_{od,t}(m) = \widehat{p}^S_{od,t}(m)/A^F_t$, we have

$$P^S_{d,t}(m) = \left[\sum_{o \in C} \chi_{od,t}(m) \left(d^S_{od} \frac{\widehat{p}^S_{od,t}(m)}{A^F_t} \right)^{1-\sigma^S} \right]^{\frac{1}{1-\sigma^S}}$$
$$= \left[\left(A^F_t \right)^{\sigma^S - 1} \sum_{o \in C} \chi_{od,t}(m) \left(d^S_{od} \widehat{p}^S_{od,t}(m) \right)^{1-\sigma^S} \right]^{\frac{1}{1-\sigma^S}}$$
$$= \frac{1}{A^F_t} \left[\sum_{o \in C} \chi_{od,t}(m) \left(d^S_{od} \widehat{p}^S_{od,t}(m) \right)^{1-\sigma^S} \right]^{\frac{1}{1-\sigma^S}}. \tag{A.51}$$

Define the stationary semiconductor variety price index by

$$\widehat{P}^S_{d,t}(m) \equiv \left[\sum_{o \in C} \chi_{od,t}(m) \left(d^S_{od} \widehat{p}^S_{od,t}(m) \right)^{1-\sigma^S} \right]^{\frac{1}{1-\sigma^S}}. \tag{A.52}$$

Then

$$P^S_{d,t}(m) = \frac{\widehat{P}^S_{d,t}(m)}{A^F_t}, \qquad \widehat{P}^S_{d,t}(m) = A^F_t P^S_{d,t}(m). \tag{A.53}$$

Step 6: The aggregate semiconductor price index also satisfies

$$\widehat{P}^S_{d,t} = A^F_t P^S_{d,t}.$$

The aggregate semiconductor price index is the geometric average across semiconductor varieties:

$$P^S_{d,t} = \exp\left(\sum_m \mu_t(m) \log P^S_{d,t}(m)\right). \tag{A.54}$$

Using $P^S_{d,t}(m) = \widehat{P}^S_{d,t}(m)/A^F_t$, we obtain

$$\begin{aligned} \log P^S_{d,t} &= \sum_m \mu_t(m) \log\left(\frac{\widehat{P}^S_{d,t}(m)}{A^F_t}\right) \\ &= \sum_m \mu_t(m) \log \widehat{P}^S_{d,t}(m) - \log A^F_t \sum_m \mu_t(m). \end{aligned} \tag{A.55}$$

Since $\sum_m \mu_t(m) = 1$,

$$\log P^S_{d,t} = \sum_m \mu_t(m) \log \widehat{P}^S_{d,t}(m) - \log A^F_t. \tag{A.56}$$

Define

$$\widehat{P}^S_{d,t} \equiv \exp\left(\sum_m \mu_t(m) \log \widehat{P}^S_{d,t}(m)\right). \tag{A.57}$$

Then

$$\log P^S_{d,t} = \log \widehat{P}^S_{d,t} - \log A^F_t, \tag{A.58}$$

or, equivalently,

$$P^S_{d,t} = \frac{\widehat{P}^S_{d,t}}{A^F_t}. \tag{A.59}$$

Therefore,

$$\boxed{\widehat{P}^S_{d,t} = A^F_t P^S_{d,t}.} \tag{A.60}$$

Step 7: The same normalization makes semiconductor expenditure stationary. Downstream semiconductor demand is written as

$$Y^S_{c,t} = z_{c,t} u_{c,t}. \tag{A.61}$$

Using $z_{c,t} = A^F_t \widehat{z}_{c,t}$,

$$Y^S_{c,t} = A^F_t \widehat{z}_{c,t} u_{c,t}. \tag{A.62}$$

Semiconductor expenditure is

$$E^S_{c,t} = P^S_{c,t} Y^S_{c,t}. \tag{A.63}$$

Substituting the previous expression for $Y^S_{c,t}$,

$$\begin{aligned} E^S_{c,t} &= P^S_{c,t} A^F_t \widehat{z}_{c,t} u_{c,t} \\ &= \left(A^F_t P^S_{c,t}\right) \widehat{z}_{c,t} u_{c,t} \\ &= \widehat{P}^S_{c,t} \widehat{z}_{c,t} u_{c,t}. \end{aligned} \tag{A.64}$$

Thus $E^S_{c,t}$ is stationary on a BGP when $\widehat{P}^S_{c,t}$, $\widehat{z}_{c,t}$, and $u_{c,t}$ are stationary.

Step 8: The downstream value function is stationary under the same normalization. The price-normalized downstream value representation is

$$V_{c,t} = P^S_{c,t} z_{c,t} \phi_{c,t} + \Omega_{c,t}. \tag{A.65}$$

Using $z_{c,t} = A^F_t \widehat{z}_{c,t}$,

$$\begin{aligned} P^S_{c,t} z_{c,t} &= P^S_{c,t} A^F_t \widehat{z}_{c,t} \\ &= \left(A^F_t P^S_{c,t}\right) \widehat{z}_{c,t} \\ &= \widehat{P}^S_{c,t} \widehat{z}_{c,t}. \end{aligned} \tag{A.66}$$

Hence the value function can be written as

$$V_{c,t} = \widehat{P}^S_{c,t}\widehat{z}_{c,t}\phi_{c,t} + \Omega_{c,t}. \tag{A.67}$$

This confirms that $\widehat{P}^S_{c,t} = A^F_t P^S_{c,t}$ is the correct price normalization associated with $\widehat{z}_{c,t} = z_{c,t}/A^F_t$.

Step 9: The transition price ratio follows immediately. Along the transition,

$$A^F_{t+\Delta t} = A^F_t \exp(g^S_t \Delta t). \tag{A.68}$$

Since

$$P^S_{c,t} = \frac{\widehat{P}^S_{c,t}}{A^F_t}, \tag{A.69}$$

we have

$$\begin{aligned}
\frac{P^S_{c,t+\Delta t}}{P^S_{c,t}} &= \frac{\widehat{P}^S_{c,t+\Delta t}/A^F_{t+\Delta t}}{\widehat{P}^S_{c,t}/A^F_t} \\
&= \frac{\widehat{P}^S_{c,t+\Delta t}}{\widehat{P}^S_{c,t}} \frac{A^F_t}{A^F_{t+\Delta t}} \\
&= \frac{\widehat{P}^S_{c,t+\Delta t}}{\widehat{P}^S_{c,t}} \exp(-g^S_t \Delta t).
\end{aligned} \tag{A.70}$$

This is the ratio that must enter the downstream transition Bellman equation and the downstream transition FOC.

Remark: Why the final-good price has a different exponent. The semiconductor price normalization has exponent one because semiconductor production is linear in semiconductor productivity:

$$y^S_{o,t} = z^S_{o,t} l^S_{o,t}. \tag{A.71}$$

Thus semiconductor marginal cost is proportional to $1/z^S_{o,t}$, and semiconductor prices scale as $1/A^F_t$.

By contrast, downstream production is

$$y_{c,t} = z^{1/(\sigma-1)}_{c,t} l_{c,t}. \tag{A.72}$$

Therefore downstream marginal cost is proportional to

$$z_{c,t}^{-1/(\sigma-1)} = \left(A_t^F \widehat{z}_{c,t}\right)^{-1/(\sigma-1)} = \left(A_t^F\right)^{-1/(\sigma-1)} \widehat{z}_{c,t}^{-1/(\sigma-1)}. \tag{A.73}$$

Hence final-good prices satisfy

$$\widehat{P}_{c,t} \equiv \left(A_t^F\right)^{1/(\sigma-1)} P_{c,t}, \tag{A.74}$$

whereas semiconductor prices satisfy

$$\widehat{P}_{c,t}^S \equiv A_t^F P_{c,t}^S. \tag{A.75}$$

The different exponents come directly from the different ways productivity enters production in the two sectors.

A.1.6 Semiconductor Production and Technology Gaps

Proposition A.1 (Semiconductor technology gaps, markups, and static profits) *Consider a semiconductor intermediate ω for which both countries can sell to destination d. Fix wages, trade costs, destination semiconductor expenditure E_d^S, and market access. Let $s_d(m) \equiv s_{Ud}^S(m) \in (0,1)$ be the U.S. share in destination d when the technology gap is $m = k_U - k_C$. The residual elasticity and markup are*

$$\varepsilon(s) = \sigma^S - (\sigma^S - 1)s, \qquad \mu^S(s) = \frac{\varepsilon(s)}{\varepsilon(s) - 1}. \tag{A.76}$$

The U.S. destination-d profit is

$$\pi_{Ud}^S(m) = \frac{s_d(m)}{\varepsilon(s_d(m))} E_d^S. \tag{A.77}$$

Moreover,

$$\frac{\partial s_d(m)}{\partial m} > 0, \qquad \frac{\partial \mu^S(s_d(m))}{\partial m} > 0, \qquad \frac{\partial}{\partial m}\left[\frac{s_d(m)}{\varepsilon(s_d(m))}\right] > 0. \tag{A.78}$$

Therefore, a larger U.S. semiconductor technology gap increases the U.S. market share, markup, and operating-profit share in every destination in which the U.S. can sell. Symmetrically, a lower m raises China's market share, markup, and operating-profit share.

Proof The U.S.-to-China delivered-price ratio in destination d is

$$\frac{d_{Ud}^S p_{Ud}^S}{d_{Cd}^S p_{Cd}^S} = \frac{d_{Ud}^S}{d_{Cd}^S}\frac{w_U^S}{w_C^S}\frac{\mu^S(s_d)}{\mu^S(1-s_d)}\lambda^{-m}. \tag{A.79}$$

The CES share odds satisfy

$$\frac{s_d}{1-s_d} = \left(\frac{d_{Ud}^S}{d_{Cd}^S}\right)^{1-\sigma^S}\left[\frac{\mu^S(s_d)}{\mu^S(1-s_d)}\frac{w_U^S}{w_C^S}\lambda^{-m}\right]^{1-\sigma^S}. \tag{A.80}$$

Taking logs and moving all terms to the left gives $H(s_d, m) = 0$, where

$$H(s_d,m) \equiv \log\frac{s_d}{1-s_d} - (1-\sigma^S)\left[\log\mu^S(s_d) - \log\mu^S(1-s_d) + \log\frac{w_U^S}{w_C^S} - m\log\lambda\right] - (1-\sigma^S)\log\frac{d_{Ud}^S}{d_{Cd}^S}.$$

Since

$$\frac{d}{ds}\log\mu^S(s) = \frac{\sigma^S - 1}{\varepsilon(s)[\varepsilon(s)-1]} > 0, \tag{A.81}$$

we have

$$H_s = \frac{1}{s_d(1-s_d)} - (1-\sigma^S)\left[\frac{d\log\mu^S(s_d)}{ds_d} + \frac{d\log\mu^S(1-s_d)}{d(1-s_d)}\right] > 0, \tag{A.82}$$

and

$$H_m = (1-\sigma^S)\log\lambda < 0. \tag{A.83}$$

The implicit-function theorem gives $\partial s_d/\partial m = -H_m/H_s > 0$. Because $\mu^S(s)$ is increasing in s, the markup also increases in m. Finally,

$$\frac{d}{ds}\left(\frac{s}{\varepsilon(s)}\right) = \frac{\varepsilon(s) - s\varepsilon'(s)}{\varepsilon(s)^2} = \frac{\sigma^S}{\varepsilon(s)^2} > 0, \tag{A.84}$$

so the operating-profit share $s_d/\varepsilon(s_d)$ is increasing in m. □

For use in the dynamic semiconductor HJB, total operating profits of an origin-o producer can

be normalized by domestic semiconductor expenditure:

$$\sum_{d\in\mathbb{C}} \pi^S_{od,t}(m) = \Pi^S_{o,t}(m) E^S_{o,t}, \qquad \Pi^S_{o,t}(m) = \sum_{d\in\mathbb{C}} \frac{s^S_{od,t}(m)}{\varepsilon^S_{od,t}(m)} \frac{E^S_{d,t}}{E^S_{o,t}}. \tag{A.85}$$

Equation (A.85) shows that semiconductor production profits are pinned down by technology-gap-dependent market shares and markups, market access $\chi_{\omega od,t}$, and destination semiconductor expenditures $E^S_{d,t}$.

A.1.7 Semiconductor Law of Motion

The law of motion of the semiconductor firm distribution is

$$\begin{aligned}
\dot{\mu}_t(m) = \frac{\mu_{t+\Delta t}(m) - \mu_t(m)}{\Delta t} &= -[e_{c,t}(m) + \iota(m, 1_{c' \text{ exports to } c}, 1_{c \text{ not in the global frontier}}) \\
&\quad + \sum_{c'\neq c} (e_{c',t}(m) + \iota(m, 1_{c \text{ exports to } c'}, 1_{c' \text{ not in the global frontier}}))]\mu_t(m) \\
&\quad + \sum_{m'} [e_{c,t}(m') + \iota(m', 1_{c' \text{ exports to } c}, 1_{c \text{ not in the global frontier}})] F_c(m', m)\mu(m') \\
&\quad + \sum_{c'\neq c} \sum_{m'} [e_{c',t}(m') + \iota(m', 1_{c \text{ exports to } c'}, 1_{c' \text{ not in the global frontier}})] F_{c'}(m', m)\mu(m').
\end{aligned} \tag{A.86}$$

A BGP requires $\dot{\mu}_t(m) = 0$ for every m.

A.1.8 Proof of Proposition 3.1

Proof We proceed in three steps. We prove the result in absolute productivity levels and then show how the stationary equations use normalized levels.

Step 1. World frontier level and normalization. For each semiconductor intermediate ω, define the frontier rung and the frontier productivity level by

$$K^F_t(\omega) \equiv \max\{k_{U,t}(\omega), k_{C,t}(\omega)\}, \qquad a^F_t(\omega) \equiv \lambda^{K^F_t(\omega)}. \tag{A.87}$$

The aggregate world semiconductor frontier is

$$A^F_t \equiv \exp\left(\int_0^1 \log a^F_t(\omega) d\omega\right), \qquad \mathcal{Z}^F_t \equiv \log A^F_t. \tag{A.88}$$

If $m > 0$, the U.S. firm is the global leader, so only a U.S. innovation raises the frontier for that

variety. If $m < 0$, China is the global leader, so only a Chinese innovation raises the frontier. If $m = 0$, either country's innovation raises the frontier. Therefore, on a BGP with stationary distribution $\mu(m)$,

$$g^S \equiv \frac{\dot{A}_t^F}{A_t^F} = \dot{\mathcal{Z}}_t^F = \left[\sum_{m>0} e_U(m)\mu(m) + \sum_{m<0} e_C(m)\mu(m) + \big(e_U(0) + e_C(0)\big)\mu(0)\right] \log\lambda. \tag{A.89}$$

The initial BGP normalization is $A_0^{F,\text{old}} = 1$. This normalization fixes the unit of semiconductor technology at the policy date; it is not an additional equilibrium equation.

Step 2. Country semiconductor productivity levels. Define the aggregate country-level semiconductor productivity indices by

$$Z_{c,t}^S \equiv \log A_{c,t}^S \equiv \int_0^1 \log z_{c,t}^S(\omega)d\omega. \tag{A.90}$$

Using the relative productivities in (A.21),

$$Z_{U,t}^S = \log A_t^F + \log\lambda \sum_{m<0} m\mu_t(m), \tag{A.91}$$

$$Z_{C,t}^S = \log A_t^F - \log\lambda \sum_{m>0} m\mu_t(m). \tag{A.92}$$

On a BGP, $\mu_t(m) = \mu(m)$ is stationary. Hence the second terms in (A.91)–(A.92) are constant and

$$\dot{Z}_{U,t}^S = \dot{Z}_{C,t}^S = \dot{\mathcal{Z}}_t^F = g^S. \tag{A.93}$$

In levels,

$$A_{U,t}^S = A_t^F \lambda^{\sum_{m<0} m\mu(m)}, \qquad A_{C,t}^S = A_t^F \lambda^{-\sum_{m>0} m\mu(m)}. \tag{A.94}$$

Thus the BGP pins down country semiconductor productivity levels relative to the world frontier, while the absolute level depends on the chosen normalization of A_t^F.

Step 3. Semiconductor prices and stationary normalized objects. For a variety with frontier level $a_t^F(\omega)$, define the variety-frontier-normalized price

$$\widehat{p}_{od,t}^S(m) \equiv a_t^F(\omega) p_{od,t}^S(\omega) = \frac{\varepsilon_{od,t}^S(m)}{\varepsilon_{od,t}^S(m) - 1} \frac{w_{o,t}^S}{\widehat{z}_o^S(m)}. \tag{A.95}$$

Hence the aggregate semiconductor price can be written as

$$P^S_{d,t} = \frac{\widehat{P}^S_{d,t}}{A^F_t}, \qquad \widehat{P}^S_{d,t} \equiv \exp\left(\sum_m \mu(m) \log \widehat{P}^S_d(m)\right), \tag{A.96}$$

where $\widehat{P}^S_d(m)$ is the CES price index computed from the normalized prices $\widehat{p}^S_{od}(m)$. On a BGP, $\widehat{P}^S_{d,t}$ is stationary because relative productivities, markups, wages, market access, and $\mu(m)$ are stationary. Therefore

$$\frac{\dot{P}^S_{d,t}}{P^S_{d,t}} = -\frac{\dot{A}^F_t}{A^F_t} = -g^S. \tag{A.97}$$

Since downstream semiconductor demand is $Y^S_{c,t} = z_{c,t}u_c = A^F_t \widehat{z}_c u_c$ with stationary $\widehat{z}_c$ and u_c, semiconductor quantities grow at g^S and semiconductor expenditures satisfy

$$P^S_{c,t} Y^S_{c,t} = \widehat{P}^S_c \widehat{z}_c u_c, \tag{A.98}$$

□

which is stationary. Semiconductor wages are stationary because the labor supplies are fixed and the semiconductor labor-market-clearing condition is written in stationary expenditure units.

Thus $g_{Z^S_U} = g_{Z^S_C} = g^S$, $g_{P^S_c} = -g^S$, $g_{Y^S_c} = g^S$, and $g_{P^S_c Y^S_c} = g_{w^S_c} = 0$. The proof also clarifies that the new BGP's absolute frontier level is not one when it is connected to a transition; it is the terminal transition value A^F_T.

Remark A.1 (Boundary-state clarification) Innovation at $m = \bar{m}$ is not allowed, so $e_U(\bar{m}) = 0$ for $\bar{m} > 0$ and $e_C(-\bar{m}) = 0$ for $-\bar{m} < 0$.

A.1.9 Downstream Production and Technology Gaps

Proposition A.2 shows that downstream profits are determined by downstream technology gaps, wages, trade costs, and destination final-good expenditure.

Lemma A.1 (Downstream shares, prices, and profits) *Fix wages* $\{w_c\}_{c\in\mathbb{C}}$, *productivities* $\{z_c\}_{c\in\mathbb{C}}$, *and downstream trade costs* $\{d_{cd}\}$. *Let* $\bar{\mu}^d \equiv \sigma/(\sigma-1)$. *For destination d, define*

$$A_{od} \equiv (d_{od} w_o)^{1-\sigma} z_o.$$

Then

$$P_d = \bar{\mu}^d \left(\sum_{o \in \mathbb{C}} A_{od} \right)^{\frac{1}{1-\sigma}}, \tag{A.99}$$

$$s_{od} = \frac{A_{od}}{\sum_{k \in \mathbb{C}} A_{kd}}, \tag{A.100}$$

$$\pi_{od} = \frac{1}{\sigma} s_{od} E_d^d, \qquad \Pi_o = \sum_{d \in \mathbb{C}} \pi_{od}. \tag{A.101}$$

Proof Step 1. The delivered price of origin o in destination d is

$$d_{od} p_o = d_{od} \bar{\mu}^d w_o z_o^{-1/(\sigma-1)}.$$

Therefore

$$(d_{od} p_o)^{1-\sigma} = (\bar{\mu}^d)^{1-\sigma} (d_{od} w_o)^{1-\sigma} z_o.$$

Substituting this expression into the CES price index gives (A.99). Step 2. CES expenditure shares are

$$s_{od} = \frac{(d_{od} p_o)^{1-\sigma}}{\sum_{k \in \mathbb{C}} (d_{kd} p_k)^{1-\sigma}},$$

which yields (A.100). Step 3. Since the markup is constant, the profit share is $1/\sigma$. Hence sales to market d equal $s_{od} E_d^d$, and operating profits equal (A.101). □

Proposition A.2 (Downstream technology gaps determine market shares and prices) *Consider two countries and fix wages and trade costs. Let $r^d = z_U / z_C$. For each destination d,*

$$\log \frac{s_{Ud}}{s_{Cd}} = \log r^d + (1-\sigma) \log \left(\frac{d_{Ud} w_U}{d_{Cd} w_C} \right). \tag{A.102}$$

Consequently,

$$\frac{\partial s_{Ud}}{\partial \log r^d} = s_{Ud}(1 - s_{Ud}) > 0, \qquad \frac{\partial s_{Cd}}{\partial \log r^d} = -s_{Ud} s_{Cd} < 0. \tag{A.103}$$

Moreover, for $o \in \{U, C\}$,

$$\frac{\partial \log P_d}{\partial \log z_o} = -\frac{s_{od}}{\sigma - 1}. \tag{A.104}$$

Thus a higher U.S. downstream technology advantage raises the U.S. downstream share in every destination and lowers final-good prices in proportion to the U.S. expenditure share in that destination.

Proof Equation (A.102) follows immediately from (A.100) because

$$\frac{s_{Ud}}{s_{Cd}} = \frac{(d_{Ud}w_U)^{1-\sigma}z_U}{(d_{Cd}w_C)^{1-\sigma}z_C}.$$

Differentiating the logit formula gives

$$\frac{\partial s_{Ud}}{\partial \log r^d} = s_{Ud}(1 - s_{Ud}),$$

and the derivative for s_{Cd} follows from $s_{Cd} = 1 - s_{Ud}$. For the price index, write

$$\log P_d = \log \bar{\mu}^d + \frac{1}{1-\sigma} \log \left(\sum_{k \in \mathbb{C}} (d_{kd}w_k)^{1-\sigma} z_k \right).$$

Differentiation with respect to $\log z_o$ yields

$$\frac{\partial \log P_d}{\partial \log z_o} = \frac{1}{1-\sigma} \frac{(d_{od}w_o)^{1-\sigma}z_o}{\sum_k (d_{kd}w_k)^{1-\sigma}z_k} = -\frac{s_{od}}{\sigma - 1}.$$ □

A.1.10 Downstream Innovator's Problem: HJB on the BGP

We guess and verify that there is a balanced growth path in which the growth rate of technology stock g is equal to the semiconductor output growth g^S (equivalent to the decline rate of semiconductor price), so the semiconductor growth determines the downstream growth. This mechanism aligns with established empirical literature (e.g., Jorgenson (2001), Jorgenson et al. (2008)), which demonstrates that falling semiconductor prices stimulate economy-wide growth.

Define the downstream innovation intensity

$$u_{c,t} \equiv \frac{Y^S_{c,t}}{z_{c,t}}. \tag{A.105}$$

Then the growth rate of the downstream productivity is

$$\frac{\dot{z}_{c,t}}{z_{c,t}} = \iota_c \left(\frac{\bar{z}_t}{z_{c,t}} - 1 \right) + \lambda^d_c u^\alpha_{c,t}. \tag{A.106}$$

The downstream innovation intensity is therefore constant on the balanced growth path.

Define

$$\phi_{c,t} \equiv \frac{1}{P^S_{c,t}} \frac{\partial V_{c,t}}{\partial z_{c,t}}, \qquad \widetilde{\pi}_{c,t} \equiv \frac{\Pi_{c,t}}{P^S_{c,t} z_{c,t}}. \tag{A.107}$$

The value-function representation consistent with BGP stationarity is

$$V_{c,t} = P^S_{c,t} z_{c,t} \phi_{c,t} + \Omega_{c,t}. \tag{A.108}$$

The downstream firm takes $P^S_{c,t}$ and $\bar{z}_t$ as aggregate objects when choosing $Y^S_{c,t}$. Hence

$$\frac{\partial V_{c,t}}{\partial z_{c,t}} = P^S_{c,t} \phi_{c,t}, \tag{A.109}$$

$$\frac{\partial V_{c,t}}{\partial t} = \dot{P}^S_{c,t} z_{c,t} \phi_{c,t} + P^S_{c,t} z_{c,t} \dot{\phi}_{c,t} + \dot{\Omega}_{c,t}. \tag{A.110}$$

Substituting (A.108) into the HJB (3.8) and using

$$\dot{z}_{c,t} = \iota_c (\bar{z}_t - z_{c,t}) + \lambda^d_c u^\alpha_{c,t} z_{c,t}$$

gives

$$\begin{aligned} &P^S_{c,t} z_{c,t} \left[R_t \phi_{c,t} - \dot{\phi}_{c,t} - \frac{\dot{P}^S_{c,t}}{P^S_{c,t}} \phi_{c,t} \right] + R_t \Omega_{c,t} - \dot{\Omega}_{c,t} \\ &\quad = \max_{u_{c,t}} \left\{ \Pi_{c,t} - P^S_{c,t} (1 - \kappa_c) u_{c,t} z_{c,t} + P^S_{c,t} \phi_{c,t} \left[\iota_c (\bar{z}_t - z_{c,t}) + \lambda^d_c u^\alpha_{c,t} z_{c,t} \right] \right\}. \end{aligned} \tag{A.111}$$

Collecting the terms proportional to the firm's own state $z_{c,t}$ and the additive spillover term gives the intensive HJB

$$R_t \phi_{c,t} - \dot{\phi}_{c,t} - \frac{\dot{P}^S_{c,t}}{P^S_{c,t}} \phi_{c,t} = \max_{u_{c,t}} \left\{ \widetilde{\pi}_{c,t} - (1 - \kappa_c) u_{c,t} + \phi_{c,t} (\lambda^d_c u^\alpha_{c,t} - \iota_c) \right\}, \tag{A.112}$$

and the additive spillover-value equation

$$R_t \Omega_{c,t} - \dot{\Omega}_{c,t} = P^S_{c,t} \phi_{c,t} \iota_c \bar{z}_t. \tag{A.113}$$

The intensive margin is pinned down by the FOC

$$1 - \kappa_c = \phi_{c,t} \lambda^d_c \alpha u^{\alpha - 1}_{c,t}, \qquad u_{c,t} = \left(\frac{\alpha \lambda^d_c \phi_{c,t}}{1 - \kappa_c} \right)^{\frac{1}{1-\alpha}}. \tag{A.114}$$

This is equivalent to (3.9) because $\partial V_{c,t}/\partial z_{c,t} = P^S_{c,t}\phi_{c,t}$.

On the BGP, $\dot{\phi}_{c,t} = 0$, $\dot{P}^S_{c,t}/P^S_{c,t} = -g$, and $\widetilde{\pi}_{c,t}$ is stationary because $P^S_{c,t}z_{c,t}$ is stationary. Therefore the stationary downstream BGP HJB is

$$\left(R + g + \iota_c - \lambda^d_c u^\alpha_c\right)\phi_c = \widetilde{\pi}_c - (1-\kappa_c)u_c, \tag{A.115}$$

with BGP FOC

$$u_c = \left(\frac{\alpha\lambda^d_c\phi_c}{1-\kappa_c}\right)^{\frac{1}{1-\alpha}}. \tag{A.116}$$

Finally, if the BGP spillover value is stationary, then (A.113) implies

$$\Omega_c = \frac{P^S_c\phi_c\iota_c\bar{z}}{R}. \tag{A.117}$$

The additive spillover value Ω_c affects firm value levels but does not enter the private FOC for u_c because each downstream firm takes $\bar{z}_t$ as given.

A.1.11 Downstream Innovator's Problem: HJB in the Transition

The transition must use the same price-normalized marginal value as the BGP. For a time step Δt, the downstream technology law of motion is

$$z_{c,t+\Delta t} = z_{c,t}\left[1 + \Delta t\left(\lambda^d_c u^\alpha_{c,t} - \iota_c\right)\right] + \iota_c\bar{z}_t\Delta t, \qquad u_{c,t} = \frac{Y^S_{c,t}}{z_{c,t}}. \tag{A.118}$$

The discrete Bellman equation is

$$V_{c,t} = \max_{u_{c,t}}\left\{\left[\Pi_{c,t} - P^S_{c,t}(1-\kappa_c)u_{c,t}z_{c,t}\right]\Delta t + e^{-R_t\Delta t}V_{c,t+\Delta t}(z_{c,t+\Delta t})\right\}. \tag{A.119}$$

Using $V_{c,t} = P^S_{c,t}z_{c,t}\phi_{c,t} + \Omega_{c,t}$ and $\widetilde{\pi}_{c,t} = \Pi_{c,t}/(P^S_{c,t}z_{c,t})$, the intensive Bellman recursion is

$$\phi_{c,t} = \max_{u_{c,t}}\left\{\Delta t\left[\widetilde{\pi}_{c,t} - (1-\kappa_c)u_{c,t}\right] + e^{-R_t\Delta t}\frac{P^S_{c,t+\Delta t}}{P^S_{c,t}}\phi_{c,t+\Delta t}\left[1 + \Delta t\left(\lambda^d_c u^\alpha_{c,t} - \iota_c\right)\right]\right\}. \tag{A.120}$$

The additive spillover-value recursion is

$$\Omega_{c,t} = e^{-R_t\Delta t}\left[P^S_{c,t+\Delta t}\phi_{c,t+\Delta t}\iota_c\bar{z}_t\Delta t + \Omega_{c,t+\Delta t}\right]. \tag{A.121}$$

The transition FOC is

$$1 - \kappa_c = e^{-R_t \Delta t} \frac{P^S_{c,t+\Delta t}}{P^S_{c,t}} \phi_{c,t+\Delta t} \lambda^d_c \alpha u^{\alpha-1}_{c,t}, \tag{A.122}$$

or equivalently

$$u_{c,t} = \left[\frac{e^{-R_t \Delta t} (P^S_{c,t+\Delta t} / P^S_{c,t}) \phi_{c,t+\Delta t} \lambda^d_c \alpha}{1 - \kappa_c} \right]^{\frac{1}{1-\alpha}}. \tag{A.123}$$

As $\Delta t \to 0$, (A.120)–(A.122) converge to (A.112) and (A.114). The term $\iota_c \bar{z}_t$ appears only in (A.121); it changes value levels and the forward law of motion for $z_{c,t}$, but it is not part of the private marginal return to $u_{c,t}$.

A.1.12 Downstream Law of Motion

Proposition A.3 (Law of motion for the downstream technology gap) *Suppose there are two countries and $\bar{z}_t = z_{U,t} + z_{C,t}$. Define*

$$a^d_{c,t} \equiv \lambda^d_c u^\alpha_{c,t}.$$

Then the downstream technology gap $r^d_t = z_{U,t}/z_{C,t}$ evolves according to

$$\frac{\dot{r}^d_t}{r^d_t} = \frac{\iota_U}{r^d_t} + a^d_{U,t} - \iota_C r^d_t - a^d_{C,t}. \tag{A.124}$$

If a^d_U and a^d_C are constant on a BGP, the stationary downstream technology gap is the unique positive root

$$r^{d,*} = \frac{a^d_U - a^d_C + \sqrt{(a^d_U - a^d_C)^2 + 4\iota_U \iota_C}}{2\iota_C}. \tag{A.125}$$

Proof Divide the downstream productivity law of motion by $z_{c,t}$. Because $\bar{z}_t = z_{U,t} + z_{C,t}$,

$$\frac{\dot{z}_{U,t}}{z_{U,t}} = \iota_U \frac{z_{C,t}}{z_{U,t}} + a^d_{U,t} = \frac{\iota_U}{r^d_t} + a^d_{U,t},$$
$$\frac{\dot{z}_{C,t}}{z_{C,t}} = \iota_C \frac{z_{U,t}}{z_{C,t}} + a^d_{C,t} = \iota_C r^d_t + a^d_{C,t}.$$

Subtracting the second growth rate from the first gives (A.124). On a BGP with common downstream

growth, $\dot{r}_t^d = 0$, so

$$\frac{\iota_U}{r^d} + a_U^d = \iota_C r^d + a_C^d.$$

Multiplying by r^d gives the quadratic equation

$$\iota_C (r^d)^2 + (a_C^d - a_U^d) r^d - \iota_U = 0.$$

The positive root is (A.125). The drift

$$\Phi(r) \equiv \frac{\iota_U}{r} + a_U^d - \iota_C r - a_C^d$$

satisfies $\Phi'(r) = -\iota_U / r^2 - \iota_C < 0$. Therefore the root is unique and locally stable. □

A.1.13 Proof of Proposition 3.2

Proof We prove in three steps.

Step 1. Stationary semiconductor expenditure requires common growth. On an interior BGP, $u_c = Y_{c,t}^S / z_{c,t}$ is stationary and strictly positive. Therefore $Y_{c,t}^S$ and $z_{c,t}$ must grow at the same rate. Proposition 3.1 implies $g_{Y_c^S} = g^S$, so

$$g_{z_c} = g_{Y_c^S} = g^S. \tag{A.126}$$

Equivalently, defining

$$\widehat{z}_{c,t} \equiv \frac{z_{c,t}}{A_t^F}, \qquad \widehat{Y}_{c,t}^S \equiv \frac{Y_{c,t}^S}{A_t^F}, \qquad \widehat{P}_{c,t}^S \equiv A_t^F P_{c,t}^S, \tag{A.127}$$

we have $\widehat{z}_{c,t}$, $\widehat{Y}_{c,t}^S$, and $\widehat{P}_{c,t}^S$ stationary on the BGP.

Step 2. Normalized downstream law of motion. Divide the raw downstream law of motion by $z_{c,t}$:

$$\frac{\dot{z}_{c,t}}{z_{c,t}} = \iota_c \left(\frac{\bar{z}_t}{z_{c,t}} - 1 \right) + \lambda_c^d u_c^\alpha. \tag{A.128}$$

Since $z_{c,t} = A_t^F \widehat{z}_{c,t}$ and $\dot{A}_t^F / A_t^F = g^S$, the normalized law is

$$\frac{\dot{\widehat{z}}_{c,t}}{\widehat{z}_{c,t}} = \iota_c \left(\frac{\widehat{z}_{U,t} + \widehat{z}_{C,t}}{\widehat{z}_{c,t}} - 1 \right) + \lambda_c^d u_c^\alpha - g^S. \tag{A.129}$$

On a BGP, $\dot{\widehat{z}}_{c,t} = 0$, so

$$g^S = \iota_c \left(\frac{\widehat{z}_U + \widehat{z}_C}{\widehat{z}_c} - 1 \right) + \lambda_c^d u_c^\alpha, \qquad c \in \{U, C\}. \tag{A.130}$$

This is the BGP equation solved numerically. It pins down the relative downstream productivity levels $\widehat{z}_c = z_{c,t}/A_t^F$, not the raw levels $z_{c,t}$.

Step 3. Downstream technology ratio and feasibility. Let $r^d = z_U/z_C = \widehat{z}_U/\widehat{z}_C$ and define $a_c^d \equiv \lambda_c^d u_c^\alpha$. With $\bar{z}_t = z_{U,t} + z_{C,t}$,

$$\frac{\dot{r}_t^d}{r_t^d} = \frac{\iota_U}{r_t^d} + a_U^d - \iota_C r_t^d - a_C^d. \tag{A.131}$$

A stationary BGP ratio satisfies

$$g^d = \frac{\iota_U}{r^{d,*}} + a_U^d = \iota_C r^{d,*} + a_C^d = g^S. \tag{A.132}$$

Because $u_c > 0$, $a_c^d > 0$. Hence

$$g^d > \frac{\iota_U}{r^{d,*}}, \qquad g^d > \iota_C r^{d,*}, \qquad (g^d)^2 > \iota_U \iota_C. \tag{A.133}$$

If $\iota_U = \iota_C = \iota$, the necessary condition becomes $\iota < g^d = g^S$.

Finally, guess and verify the detrended variables that are constant on the BGP:

$$\tilde{z}_c = z_{c,t} e^{-gt}, \qquad \tilde{P}_c = P_{c,t} e^{gt/(\sigma-1)}, \qquad \tilde{Y}_c = Y_{c,t} e^{-gt/(\sigma-1)}. \tag{A.134}$$

□

A.1.14 Two-Sector Trade balance Linkage

Proposition A.4 (Two-sector trade balance linkage) *Let the bilateral trade balance of country c against c′ be*

$$TB_{cc',t} \equiv EX_{cc',t}^d - EX_{c'c,t}^d + EX_{cc',t}^S - EX_{c'c,t}^S. \tag{A.135}$$

The balance-of-payments condition implies

$$TB_{cc',t} + R_t B_{c,t} - \dot{B}_{c,t} = 0. \tag{A.136}$$

Therefore, if bond positions are fixed on a BGP, any export control that directly reduces $EX^S_{Uc,t}$ must be absorbed by some combination of: (i) a change in downstream exports $EX^d_{Uc,t} - EX^d_{cU,t}$; (ii) a change in semiconductor imports; and (iii) general-equilibrium movements in wages, prices, and expenditures that alter both sectors' trade shares.

Proof The result is a direct rearrangement of the model's BOP condition:

$$EX^d_{cc',t} - EX^d_{c'c,t} + EX^S_{cc',t} - EX^S_{c'c,t} + R_t B_{c,t} - \dot{B}_{c,t} = 0.$$

If $B_{c,t} = \bar{B}_c$ on a BGP, then $\dot{B}_{c,t} = 0$. Hence a fall in one component of semiconductor net exports must be offset by changes in the remaining terms. Since downstream trade shares depend on z_U/z_C, downstream wages, and trade costs, and semiconductor trade shares depend on m, semiconductor wages, and market access, the two sectors cannot be analyzed independently in general equilibrium.□

A.2 Equilibrium Conditions in World-Semiconductor-Frontier-Detrended Variables

This subsection rewrites the baseline equilibrium conditions using the world semiconductor technology frontier as the common trend. Let

$$A^F_t \equiv \exp\left(\int_0^1 \log a^F_t(\omega) d\omega\right), \qquad a^F_t(\omega) \equiv \lambda^{K^F_t(\omega)}, \qquad K^F_t(\omega) \equiv \max\{k_{U,t}(\omega), k_{C,t}(\omega)\}. \tag{A.137}$$

The instantaneous growth rate of the world semiconductor frontier is

$$g^S_t \equiv \frac{\dot{A}^F_t}{A^F_t}. \tag{A.138}$$

The key normalization is that all stationary variables are measured relative to A^F_t. The initial BGP normalization is

$$A^{F,\text{old}}_0 = 1. \tag{A.139}$$

The new BGP may be solved as a stand-alone stationary system with an arbitrary normalization, but when it is connected to a transition path ending at T, its frontier level is inherited from the transition:

$$A^{F,\text{new}|T}_T = A^F_T \neq 1 \quad \text{in general.} \tag{A.140}$$

A.2.1 Detrended Variables and Raw-Level Recovery

For downstream productivity, define

$$\widehat{z}_{c,t} \equiv \frac{z_{c,t}}{A_t^F}, \qquad z_{c,t} = A_t^F \widehat{z}_{c,t}, \qquad \widehat{\bar{z}}_t \equiv \sum_{c \in C} \widehat{z}_{c,t}. \tag{A.141}$$

For downstream final-good prices and quantities, define

$$\widehat{P}_{c,t} \equiv (A_t^F)^{\frac{1}{\sigma-1}} P_{c,t}, \qquad \widehat{p}_{c,t} \equiv (A_t^F)^{\frac{1}{\sigma-1}} p_{c,t}, \tag{A.142}$$

and

$$\widehat{Y}_{c,t} \equiv \frac{Y_{c,t}}{(A_t^F)^{\frac{1}{\sigma-1}}}, \qquad \widehat{C}_{c,t} \equiv \frac{C_{c,t}}{(A_t^F)^{\frac{1}{\sigma-1}}}. \tag{A.143}$$

Hence final-good expenditure is stationary:

$$E_{c,t} \equiv P_{c,t} Y_{c,t} = \widehat{P}_{c,t} \widehat{Y}_{c,t}. \tag{A.144}$$

For semiconductor prices, define

$$\widehat{P}^S_{c,t} \equiv A_t^F P^S_{c,t}, \qquad P^S_{c,t} = \frac{\widehat{P}^S_{c,t}}{A_t^F}. \tag{A.145}$$

At the variety level, if $m = k_U - k_C$, the frontier-normalized semiconductor productivities are

$$\widehat{z}^S_U(m) = \lambda^{\min\{m,0\}}, \qquad \widehat{z}^S_C(m) = \lambda^{-\max\{m,0\}}. \tag{A.146}$$

Thus a country at the frontier has relative semiconductor productivity one, and a laggard is below the frontier by the appropriate number of rungs.

For semiconductor quantities, define

$$\widehat{Y}^S_{c,t} \equiv \frac{Y^S_{c,t}}{A_t^F}. \tag{A.147}$$

The downstream innovation intensity is

$$u_{c,t} \equiv \frac{Y^S_{c,t}}{z_{c,t}} = \frac{\widehat{Y}^S_{c,t}}{\widehat{z}_{c,t}}, \qquad \widehat{Y}^S_{c,t} = \widehat{z}_{c,t} u_{c,t}. \tag{A.148}$$

Therefore semiconductor expenditure is stationary:

$$E^S_{c,t} \equiv P^S_{c,t} Y^S_{c,t} = \widehat{P}^S_{c,t} \widehat{z}_{c,t} u_{c,t}. \tag{A.149}$$

The semiconductor R&D shifter is

$$Q^S_{c,t} = (A^F_t)^{\frac{1}{\sigma-1}}, \qquad P_{c,t} Q^S_{c,t} = \widehat{P}_{c,t}. \tag{A.150}$$

Hence define the detrended semiconductor R&D quantity

$$\widehat{RD}^S_c(e) \equiv \frac{RD^S_{c,t}(e)}{Q^S_{c,t}} = \frac{\lambda^S_c (1-\kappa^S_c)}{\gamma} e^{\gamma}. \tag{A.151}$$

The corresponding R&D expenditure is

$$P_{c,t} RD^S_{c,t}(e) = \widehat{P}_{c,t} \frac{\lambda^S_c (1-\kappa^S_c)}{\gamma} e^{\gamma}. \tag{A.152}$$

A.2.2 BGP Equilibrium in Detrended Variables

On a BGP, $g^S_t = g^S$ is constant, $A^F_t = A^F_0 \exp(g^S t)$, and all hatted variables are stationary. The BGP equilibrium is characterized by the following conditions.

World semiconductor frontier growth. Let $\mu(m)$ denote the stationary distribution of technology gaps. Then

$$g^S = \left[\sum_{m>0} e_U(m)\mu(m) + \sum_{m<0} e_C(m)\mu(m) + \big(e_U(0) + e_C(0)\big)\mu(0) \right] \log \lambda. \tag{A.153}$$

The country-level aggregate semiconductor productivity indices are recovered from

$$A^S_{U,t} = A^F_t \lambda^{\sum_{m<0} m\mu(m)}, \tag{A.154}$$

$$A^S_{C,t} = A^F_t \lambda^{-\sum_{m>0} m\mu(m)}. \tag{A.155}$$

Thus the BGP pins down country semiconductor productivities relative to A^F_t; absolute levels are recovered only after choosing the frontier normalization.

Semiconductor static block. For origin o, destination d, and gap state m, the detrended semiconductor intermediate price is

$$\widehat{p}^{S}_{od}(m) = \frac{\varepsilon^{S}_{od}(m)}{\varepsilon^{S}_{od}(m) - 1} \frac{w^{S}_{o}}{\widehat{z}^{S}_{o}(m)}. \tag{A.156}$$

The destination-d semiconductor price index for gap state m is

$$\widehat{P}^{S}_{d}(m) = \left[\sum_{o \in C} \chi_{od}(m) \left(d^{S}_{od} \widehat{p}^{S}_{od}(m) \right)^{1-\sigma^{S}} \right]^{\frac{1}{1-\sigma^{S}}}, \tag{A.157}$$

where $\chi_{od}(m) \in \{0, 1\}$ is the export-control or market-access indicator. The expenditure share and residual elasticity are

$$s^{S}_{od}(m) = \chi_{od}(m) \left(\frac{d^{S}_{od} \widehat{p}^{S}_{od}(m)}{\widehat{P}^{S}_{d}(m)} \right)^{1-\sigma^{S}}, \tag{A.158}$$

$$\varepsilon^{S}_{od}(m) = s^{S}_{od}(m) + \sigma^{S} \left(1 - s^{S}_{od}(m) \right). \tag{A.159}$$

The aggregate detrended semiconductor price index is

$$\widehat{P}^{S}_{d} = \exp \left(\sum_{m} \mu(m) \log \widehat{P}^{S}_{d}(m) \right). \tag{A.160}$$

Total operating profits of an origin-o semiconductor producer in state m are

$$\pi^{S}_{o}(m) = \sum_{d \in C} \frac{s^{S}_{od}(m)}{\varepsilon^{S}_{od}(m)} E^{S}_{d}. \tag{A.161}$$

Semiconductor labor-market clearing. For each origin country o,

$$w^{S}_{o} L^{S}_{o} = \sum_{d \in C} \sum_{m} \frac{\varepsilon^{S}_{od}(m) - 1}{\varepsilon^{S}_{od}(m)} s^{S}_{od}(m) E^{S}_{d} \mu(m). \tag{A.162}$$

Semiconductor values and innovation. Let $o' \neq o$. Define the innovation-gain operator

$$\Delta^{S}_{o|j}(m) \equiv \sum_{m'} F_{j}(m, m') V^{S}_{o}(m') - V^{S}_{o}(m), \qquad j \in \{o, o'\}. \tag{A.163}$$

Let $\iota_j^S(m)$ denote the knowledge-spillover arrival rate for country j in state m, and define the total transition arrival rate

$$a_j(m) \equiv e_j(m) + \iota_j^S(m). \tag{A.164}$$

The stationary semiconductor HJB is

$$RV_o^S(m) = \max_{e\in[0,\bar{e}]} \Bigg\{ \pi_o^S(m) - \widehat{P}_o \frac{\lambda_o^S(1-\kappa_o^S)}{\gamma} e^{\gamma} + \big(e + \iota_o^S(m)\big)\Delta_{o|o}^S(m) + a_{o'}(m)\Delta_{o|o'}^S(m) \Bigg\}. \tag{A.165}$$

The semiconductor innovation policy satisfies

$$e_o(m) = \left[\frac{\Delta_{o|o}^S(m)}{\lambda_o^S(1-\kappa_o^S)\widehat{P}_o} \right]^{\frac{1}{\gamma-1}}, \tag{A.166}$$

with projection onto $[0, \bar{e}]$:

$$e_o(m) = \min\left\{ \bar{e}, \max\left[0, \left(\frac{\Delta_{o|o}^S(m)}{\lambda_o^S(1-\kappa_o^S)\widehat{P}_o} \right)^{\frac{1}{\gamma-1}} \right] \right\}. \tag{A.167}$$

Stationary distribution of semiconductor gaps. The stationary distribution satisfies, for every m,

$$0 = -\big[a_U(m) + a_C(m)\big]\mu(m) + \sum_{m'} a_U(m')F_U(m',m)\mu(m') + \sum_{m'} a_C(m')F_C(m',m)\mu(m'), \tag{A.168}$$

with

$$\sum_m \mu(m) = 1, \qquad \mu(m) \geq 0. \tag{A.169}$$

Downstream static block. The detrended downstream producer price is

$$\widehat{p}_o = \frac{\sigma}{\sigma-1} w_o \widehat{z}_o^{-\frac{1}{\sigma-1}}. \tag{A.170}$$

The detrended final-good price index in destination d is

$$\widehat{P}_d = \left[\sum_{o\in C}\left(d_{od}\widehat{p}_o\right)^{1-\sigma}\right]^{\frac{1}{1-\sigma}} = \frac{\sigma}{\sigma-1}\left[\sum_{o\in C}\left(d_{od}w_o\right)^{1-\sigma}\widehat{z}_o\right]^{\frac{1}{1-\sigma}}. \tag{A.171}$$

The downstream expenditure share is

$$s_{od} = \left(\frac{d_{od}\widehat{p}_o}{\widehat{P}_d}\right)^{1-\sigma} = \frac{\left(d_{od}w_o\right)^{1-\sigma}\widehat{z}_o}{\sum_{k\in C}\left(d_{kd}w_k\right)^{1-\sigma}\widehat{z}_k}. \tag{A.172}$$

Destination expenditure and output satisfy

$$E_d = \widehat{P}_d\widehat{Y}_d, \qquad \widehat{Y}_d = \frac{E_d}{\widehat{P}_d}. \tag{A.173}$$

Operating profits of the downstream producer in origin o are

$$\Pi_o = \frac{1}{\sigma}\sum_{d\in C} s_{od}E_d. \tag{A.174}$$

Downstream labor-market clearing. Normalize the U.S. downstream wage by

$$w_U = 1. \tag{A.175}$$

For each origin o,

$$w_oL_o = \frac{\sigma-1}{\sigma}\sum_{d\in C} s_{od}E_d = (\sigma-1)\Pi_o. \tag{A.176}$$

Downstream productivity law. The raw law of motion is

$$\dot{z}_{c,t} = \iota_c(\bar{z}_t - z_{c,t}) + \lambda_c^d u_{c,t}^{\alpha} z_{c,t}. \tag{A.177}$$

Using $z_{c,t} = A_t^F\widehat{z}_{c,t}$, the detrended law is

$$\dot{\widehat{z}}_{c,t} = \iota_c(\widehat{\bar{z}}_t - \widehat{z}_{c,t}) + \lambda_c^d u_{c,t}^{\alpha}\widehat{z}_{c,t} - g^S\widehat{z}_{c,t}. \tag{A.178}$$

On a BGP, $\dot{\widehat{z}}_{c,t} = 0$, so

$$g^S = \iota_c \left(\frac{\widehat{\bar{z}}}{\widehat{z}_c} - 1 \right) + \lambda_c^d u_c^\alpha, \qquad c \in C. \tag{A.179}$$

Downstream values and innovation. Define the price-normalized marginal value

$$\phi_c \equiv \frac{1}{P_{c,t}^S} \frac{\partial V_{c,t}}{\partial z_{c,t}}, \tag{A.180}$$

and the stationary normalized downstream profit

$$\widetilde{\pi}_c \equiv \frac{\Pi_c}{P_{c,t}^S z_{c,t}} = \frac{\Pi_c}{\widehat{P}_c^S \widehat{z}_c}. \tag{A.181}$$

The value-function representation is

$$V_{c,t} = P_{c,t}^S z_{c,t} \phi_c + \Omega_c = \widehat{P}_c^S \widehat{z}_c \phi_c + \Omega_c. \tag{A.182}$$

The stationary downstream HJB is

$$\left(R + g^S + \iota_c - \lambda_c^d u_c^\alpha\right) \phi_c = \widetilde{\pi}_c - (1 - \kappa_c) u_c. \tag{A.183}$$

The downstream innovation FOC is

$$1 - \kappa_c = \phi_c \lambda_c^d \alpha u_c^{\alpha - 1}, \qquad u_c = \left(\frac{\alpha \lambda_c^d \phi_c}{1 - \kappa_c} \right)^{\frac{1}{1-\alpha}}. \tag{A.184}$$

The additive spillover-value component is

$$\Omega_c = \frac{\widehat{P}_c^S \phi_c \iota_c \widehat{\bar{z}}}{R}. \tag{A.185}$$

This term affects value levels but not the private downstream innovation FOC because the downstream firm takes $\widehat{\bar{z}}$ as given.

Final-good resource constraint and consumption. The detrended final-good resource constraint is

$$\widehat{C}_c = \widehat{Y}_c - \sum_m \widehat{RD}_c^S(e_c(m)) \mu(m), \tag{A.186}$$

where

$$\widehat{RD}_c^S(e_c(m)) = \frac{\lambda_c^S(1-\kappa_c^S)}{\gamma} e_c(m)^\gamma. \tag{A.187}$$

Households, bonds, and the balance of payments. Since $P_{c,t}C_{c,t} = \widehat{P}_c\widehat{C}_c$, nominal consumption expenditure is stationary. The Euler equation is

$$R = \rho + \eta(B_c - \bar{B}_c). \tag{A.188}$$

On the BGP with fixed bond positions,

$$B_c = \bar{B}_c, \qquad \sum_{c\in C} \bar{B}_c = 0, \qquad R = \rho. \tag{A.189}$$

Downstream and semiconductor exports are

$$EX_{od} = s_{od}E_d, \tag{A.190}$$

$$EX_{od}^S = \sum_m s_{od}^S(m)E_d^S\mu(m). \tag{A.191}$$

For country c, with $c' \neq c$, the BGP balance-of-payments condition is

$$EX_{cc'} - EX_{c'c} + EX_{cc'}^S - EX_{c'c}^S + R\bar{B}_c = 0. \tag{A.192}$$

Stationary dividends and household budget. The stationary dividend income of country c is

$$D_c = \Pi_c - (1-\kappa_c)E_c^S + \sum_m \left[\pi_c^S(m) - \widehat{P}_c\widehat{RD}_c^S(e_c(m))\right]\mu(m). \tag{A.193}$$

The stationary household budget constraint is

$$\widehat{P}_c\widehat{C}_c + \frac{\eta}{2}(B_c - \bar{B}_c)^2 = w_cL_c + w_c^SL_c^S + D_c + RB_c + Tr_c. \tag{A.194}$$

With the transfer rule rebating portfolio adjustment costs and financing subsidies, this condition is consistent with the resource constraint and the balance of payments.

A.2.3 Transition Equilibrium in Detrended Variables

The transition is solved on a grid $t_n = n\Delta t$, $n = 0, 1, \ldots, N$, with $t_N = T$. R_n is the one-period net interest rate between t_n and t_{n+1}. Hence R_n prices continuation values from n to $n+1$, enters bond accumulation from $B_{c,n}$ to $B_{c,n+1}$, and is pinned down by the Euler equation using nominal consumption-expenditure growth from n to $n+1$. The frontier is normalized at the initial date:

$$A_0^F = 1. \tag{A.195}$$

At each date, the world semiconductor frontier growth rate is

$$g_n^S = \left[\sum_{m>0} e_{U,n}(m)\mu_n(m) + \sum_{m<0} e_{C,n}(m)\mu_n(m) + \big(e_{U,n}(0) + e_{C,n}(0)\big)\mu_n(0)\right] \log\lambda, \tag{A.196}$$

and the frontier level evolves according to

$$A_{n+1}^F = A_n^F \exp(g_n^S \Delta t). \tag{A.197}$$

Thus

$$A_N^F = \exp\left(\sum_{n=0}^{N-1} g_n^S \Delta t\right), \qquad A_T^{F,\text{new}|T} = A_N^F. \tag{A.198}$$

Transition variables. The transition carries

$$\widehat{z}_{c,n} = \frac{z_{c,n}}{A_n^F}, \qquad \widehat{P}_{c,n}^S = A_n^F P_{c,n}^S, \qquad \widehat{P}_{c,n} = (A_n^F)^{\frac{1}{\sigma-1}} P_{c,n}. \tag{A.199}$$

Raw variables are recovered from

$$z_{c,n} = A_n^F \widehat{z}_{c,n}, \qquad P_{c,n}^S = \frac{\widehat{P}_{c,n}^S}{A_n^F}, \qquad P_{c,n} = \frac{\widehat{P}_{c,n}}{(A_n^F)^{\frac{1}{\sigma-1}}}. \tag{A.200}$$

Final-good and consumption quantities are recovered from

$$Y_{c,n} = (A_n^F)^{\frac{1}{\sigma-1}} \widehat{Y}_{c,n}, \qquad C_{c,n} = (A_n^F)^{\frac{1}{\sigma-1}} \widehat{C}_{c,n}. \tag{A.201}$$

Transition static downstream block. Given $\widehat{z}_{o,n}$ and wages $w_{o,n}$, with $w_{U,n} = 1$,

$$\widehat{p}_{o,n} = \frac{\sigma}{\sigma - 1} w_{o,n} \widehat{z}_{o,n}^{-\frac{1}{\sigma-1}}, \tag{A.202}$$

$$\widehat{P}_{d,n} = \left[\sum_{o \in C} \left(d_{od} \widehat{p}_{o,n} \right)^{1-\sigma} \right]^{\frac{1}{1-\sigma}} = \frac{\sigma}{\sigma - 1} \left[\sum_{o \in C} \left(d_{od} w_{o,n} \right)^{1-\sigma} \widehat{z}_{o,n} \right]^{\frac{1}{1-\sigma}}, \tag{A.203}$$

and

$$s_{od,n} = \left(\frac{d_{od} \widehat{p}_{o,n}}{\widehat{P}_{d,n}} \right)^{1-\sigma} = \frac{\left(d_{od} w_{o,n} \right)^{1-\sigma} \widehat{z}_{o,n}}{\sum_{k \in C} \left(d_{kd} w_{k,n} \right)^{1-\sigma} \widehat{z}_{k,n}}. \tag{A.204}$$

Final-good expenditure and detrended output satisfy

$$E_{d,n} = \widehat{P}_{d,n} \widehat{Y}_{d,n}, \qquad \widehat{Y}_{d,n} = \frac{E_{d,n}}{\widehat{P}_{d,n}}. \tag{A.205}$$

Downstream profits are

$$\Pi_{o,n} = \frac{1}{\sigma} \sum_{d \in C} s_{od,n} E_{d,n}. \tag{A.206}$$

Transition downstream labor-market clearing. For each origin o,

$$w_{o,n} L_o = \frac{\sigma - 1}{\sigma} \sum_{d \in C} s_{od,n} E_{d,n} = (\sigma - 1) \Pi_{o,n}. \tag{A.207}$$

Transition static semiconductor block. For origin o, destination d, and gap state m,

$$\widehat{p}^{S}_{od,n}(m) = \frac{\varepsilon^{S}_{od,n}(m)}{\varepsilon^{S}_{od,n}(m) - 1} \frac{w^{S}_{o,n}}{\widehat{z}^{S}_{o}(m)}. \tag{A.208}$$

The detrended semiconductor price index by gap state is

$$\widehat{P}^{S}_{d,n}(m) = \left[\sum_{o \in C} \chi_{od,n}(m) \left(d^{S}_{od} \widehat{p}^{S}_{od,n}(m) \right)^{1-\sigma^{S}} \right]^{\frac{1}{1-\sigma^{S}}}. \tag{A.209}$$

The semiconductor shares and residual elasticities are

$$s^S_{od,n}(m) = \chi_{od,n}(m)\left(\frac{d^S_{od}\widehat{p}^S_{od,n}(m)}{\widehat{P}^S_{d,n}(m)}\right)^{1-\sigma^S}, \tag{A.210}$$

$$\varepsilon^S_{od,n}(m) = s^S_{od,n}(m) + \sigma^S\big(1 - s^S_{od,n}(m)\big). \tag{A.211}$$

The aggregate detrended semiconductor price index is

$$\widehat{P}^S_{d,n} = \exp\left(\sum_m \mu_n(m)\log\widehat{P}^S_{d,n}(m)\right). \tag{A.212}$$

Total operating profits of an origin-o semiconductor producer in state m are

$$\pi^S_{o,n}(m) = \sum_{d\in C}\frac{s^S_{od,n}(m)}{\varepsilon^S_{od,n}(m)}E^S_{d,n}. \tag{A.213}$$

Transition semiconductor labor-market clearing. For each origin o,

$$w^S_{o,n}L^S_o = \sum_{d\in C}\sum_m \frac{\varepsilon^S_{od,n}(m)-1}{\varepsilon^S_{od,n}(m)}s^S_{od,n}(m)E^S_{d,n}\mu_n(m). \tag{A.214}$$

Transition downstream semiconductor demand. The detrended semiconductor quantity used by the downstream firm is

$$\widehat{Y}^S_{c,n} = \widehat{z}_{c,n}u_{c,n}. \tag{A.215}$$

Hence semiconductor expenditure is

$$E^S_{c,n} = P^S_{c,n}Y^S_{c,n} = \widehat{P}^S_{c,n}\widehat{z}_{c,n}u_{c,n}. \tag{A.216}$$

Transition downstream productivity law. The raw law of motion is

$$z_{c,n+1} = z_{c,n}\left[1 + \Delta t\big(\lambda^d_c u^\alpha_{c,n} - \iota_c\big)\right] + \iota_c\bar{z}_n\Delta t. \tag{A.217}$$

Using $z_{c,n} = A^F_n\widehat{z}_{c,n}$ and $A^F_{n+1} = A^F_n\exp(g^S_n\Delta t)$, the detrended law used in computation is

$$\widehat{z}_{c,n+1} = \exp(-g^S_n\Delta t)\left\{\widehat{z}_{c,n}\left[1 + \Delta t\big(\lambda^d_c u^\alpha_{c,n} - \iota_c\big)\right] + \iota_c\widehat{\bar{z}}_n\Delta t\right\}. \tag{A.218}$$

Transition downstream value recursion and FOC. Define

$$\widetilde{\pi}_{c,n} \equiv \frac{\Pi_{c,n}}{\widehat{P}^S_{c,n}\widehat{z}_{c,n}}. \tag{A.219}$$

The actual semiconductor price ratio is

$$\frac{P^S_{c,n+1}}{P^S_{c,n}} = \exp(-g^S_n\Delta t)\frac{\widehat{P}^S_{c,n+1}}{\widehat{P}^S_{c,n}}. \tag{A.220}$$

Using

$$V_{c,n} = P^S_{c,n}z_{c,n}\phi_{c,n} + \Omega_{c,n} = \widehat{P}^S_{c,n}\widehat{z}_{c,n}\phi_{c,n} + \Omega_{c,n}, \tag{A.221}$$

the intensive downstream Bellman recursion is

$$\begin{aligned}\phi_{c,n} = {} & \Delta t\left[\widetilde{\pi}_{c,n} - (1-\kappa_c)u_{c,n}\right] \\ & + \exp(-R_n\Delta t)\exp(-g^S_n\Delta t)\frac{\widehat{P}^S_{c,n+1}}{\widehat{P}^S_{c,n}}\phi_{c,n+1}\left[1 + \Delta t\left(\lambda^d_c u^\alpha_{c,n} - \iota_c\right)\right].\end{aligned} \tag{A.222}$$

The transition FOC is

$$1 - \kappa_c = \exp(-R_n\Delta t)\exp(-g^S_n\Delta t)\frac{\widehat{P}^S_{c,n+1}}{\widehat{P}^S_{c,n}}\phi_{c,n+1}\lambda^d_c\alpha u^{\alpha-1}_{c,n}, \tag{A.223}$$

or equivalently

$$u_{c,n} = \left[\frac{\exp(-R_n\Delta t)\exp(-g^S_n\Delta t)\left(\widehat{P}^S_{c,n+1}/\widehat{P}^S_{c,n}\right)\phi_{c,n+1}\lambda^d_c\alpha}{1-\kappa_c}\right]^{\frac{1}{1-\alpha}}. \tag{A.224}$$

The additive spillover-value recursion is

$$\Omega_{c,n} = \exp(-R_n\Delta t)\left[\exp(-g^S_n\Delta t)\widehat{P}^S_{c,n+1}\phi_{c,n+1}\iota_c\widehat{\bar{z}}_n\Delta t + \Omega_{c,n+1}\right]. \tag{A.225}$$

Transition semiconductor value recursion and FOC. Define

$$\Delta^S_{o,n+1|j}(m) \equiv \sum_{m'} F_j(m,m')V^S_{o,n+1}(m') - V^S_{o,n+1}(m), \qquad j \in \{U, C\}. \tag{A.226}$$

Let

$$a_{j,n}(m) \equiv e_{j,n}(m) + \iota^S_{j,n}(m). \tag{A.227}$$

The semiconductor Bellman recursion is

$$V^S_{o,n}(m) = \max_{e\in[0,\bar{e}]}\Bigg\{\Delta t\left[\pi^S_{o,n}(m) - \widehat{P}_{o,n}\frac{\lambda^S_o(1-\kappa^S_o)}{\gamma}e^\gamma\right] + \exp(-R_n\Delta t)\left[V^S_{o,n+1}(m) + \Delta t\left\{\left(e+\iota^S_{o,n}(m)\right)\Delta^S_{o,n+1|o}(m) + a_{o',n}(m)\Delta^S_{o,n+1|o'}(m)\right\}\right]\Bigg\}. \tag{A.228}$$

The innovation policy is

$$e_{o,n}(m) = \min\left\{\bar{e}, \max\left[0, \left(\frac{\exp(-R_n\Delta t)\Delta^S_{o,n+1|o}(m)}{\lambda^S_o(1-\kappa^S_o)\widehat{P}_{o,n}}\right)^{\frac{1}{\gamma-1}}\right]\right\}. \tag{A.229}$$

Transition distribution law. The semiconductor technology-gap distribution evolves according to

$$\mu_{n+1}(m) = \mu_n(m) + \Delta t\Bigg\{-\left[a_{U,n}(m)+a_{C,n}(m)\right]\mu_n(m) + \sum_{m'}a_{U,n}(m')F_U(m',m)\mu_n(m') + \sum_{m'}a_{C,n}(m')F_C(m',m)\mu_n(m')\Bigg\}, \tag{A.230}$$

with

$$\sum_m \mu_n(m) = 1, \qquad \mu_n(m) \geq 0 \quad \text{for all } n. \tag{A.231}$$

Transition final-good resource constraint and consumption. The detrended R&D quantity is

$$\widehat{RD}^S_{c,n}(e) = \frac{\lambda^S_c(1-\kappa^S_c)}{\gamma}e^\gamma. \tag{A.232}$$

The detrended final-good resource constraint is

$$\widehat{C}_{c,n} = \widehat{Y}_{c,n} - \sum_{m} \widehat{RD}^{S}_{c,n}\big(e_{c,n}(m)\big)\mu_n(m), \qquad \widehat{Y}_{c,n} = \frac{E_{c,n}}{\widehat{P}_{c,n}}. \tag{A.233}$$

Raw consumption is recovered as

$$C_{c,n} = (A^F_n)^{\frac{1}{\sigma-1}}\widehat{C}_{c,n}. \tag{A.234}$$

Transition exports, bonds, and balance of payments. Downstream and semiconductor exports are

$$EX_{od,n} = s_{od,n}E_{d,n}, \tag{A.235}$$

$$EX^{S}_{od,n} = \sum_{m} s^{S}_{od,n}(m)E^{S}_{d,n}\mu_n(m). \tag{A.236}$$

For country c, with $c' \neq c$, net exports are

$$NX_{c,n} = EX_{cc',n} - EX_{c'c,n} + EX^{S}_{cc',n} - EX^{S}_{c'c,n}. \tag{A.237}$$

The bond law of motion is

$$B_{c,n+1} = B_{c,n} + \Delta t\left[NX_{c,n} + R_n B_{c,n}\right], \tag{A.238}$$

with bond-market clearing

$$\sum_{c\in C} B_{c,n} = 0 \qquad \text{for every } n. \tag{A.239}$$

Equivalently, the period-n balance-of-payments residual is

$$NX_{c,n} + R_n B_{c,n} - \frac{B_{c,n+1} - B_{c,n}}{\Delta t} = 0. \tag{A.240}$$

Transition Euler equations. Because

$$P_{c,n}C_{c,n} = \widehat{P}_{c,n}\widehat{C}_{c,n}, \tag{A.241}$$

the Euler equation can be written entirely in detrended variables:

$$R_n = \rho + \eta(B_{c,n} - \bar{B}_c) + \frac{1}{\Delta t}\log\left(\frac{\widehat{P}_{c,n+1}\widehat{C}_{c,n+1}}{\widehat{P}_{c,n}\widehat{C}_{c,n}}\right), \qquad c \in C. \tag{A.242}$$

Transition dividends and household budget. Stationary dividends are

$$D_{c,n} = \Pi_{c,n} - (1-\kappa_c)E^S_{c,n} + \sum_m \left[\pi^S_{c,n}(m) - \widehat{P}_{c,n}\widehat{RD}^S_{c,n}\big(e_{c,n}(m)\big)\right]\mu_n(m). \tag{A.243}$$

The household budget constraint in stationary units is

$$\widehat{P}_{c,n}\widehat{C}_{c,n} + \frac{B_{c,n+1} - B_{c,n}}{\Delta t} + \frac{\eta}{2}(B_{c,n} - \bar{B}_c)^2 = w_{c,n}L_c + w^S_{c,n}L^S_c + D_{c,n} + R_n B_{c,n} + Tr_{c,n}. \tag{A.244}$$

Boundary conditions for transition. The transition starts from the initial BGP:

$$A^F_0 = 1, \qquad \mu_0(m) = \mu^{\text{old}}(m), \qquad \widehat{z}_{c,0} = \widehat{z}^{\text{old}}_c, \qquad B_{c,0} = \bar{B}^{\text{old}}_c. \tag{A.245}$$

The backward-looking value variables use terminal continuation values from the new BGP:

$$V^S_{c,N}(m) = V^{S,\text{new}}_c(m), \qquad \phi_{c,N} = \phi^{\text{new}}_c. \tag{A.246}$$

The terminal state restrictions are imposed in detrended variables:

$$\mu_N(m) \approx \mu^{\text{new}}(m), \qquad \widehat{z}_{c,N} \approx \widehat{z}^{\text{new}}_c, \qquad B_{c,N} \approx \bar{B}^{\text{new}}_c. \tag{A.247}$$

The corresponding raw terminal levels are

$$z_{c,N} = A^F_N \widehat{z}^{\text{new}}_c, \qquad A^{F,\text{new}|T}_T = A^F_N. \tag{A.248}$$

Summary of the detrended transition equilibrium. A transition equilibrium in world-semiconductor-frontier-detrended variables is a sequence

$$\left\{w_{c,n}, w^S_{c,n}, R_n, B_{c,n}, \widehat{z}_{c,n}, \widehat{P}_{c,n}, \widehat{P}^S_{c,n}, E_{c,n}, E^S_{c,n}, \widehat{C}_{c,n}, \phi_{c,n}, \Omega_{c,n}, u_{c,n}, V^S_{c,n}(m), e_{c,n}(m), \mu_n(m)\right\}_{c,m,n} \tag{A.249}$$

such that equations (A.196)–(A.247) hold for every n. Raw levels are not equilibrium unknowns; they are recovered from (A.200), (A.201), and (A.248) after the detrended equilibrium path has

been solved.

A.3 Model Mechanisms: Analytical Characterizations

This section analytically characterizes the effects of U.S. semiconductor controls on the U.S. and China.

A.3.1 Effects on Semiconductor Innovation and Technology Gaps

This section shows that U.S. semiconductor controls could raise the U.S. innovation prize by reducing knowledge diffusion to China and slowing down China's catch-up, but may not raise semiconductor growth.

Proposition A.5 (A loss of spillovers raises the leader's innovation prize) *Consider a partial-equilibrium two-state approximation for a U.S. semiconductor firm that is either a leader L or neck-and-neck N. Let the flow profit advantage be $\pi_L - \pi_N > 0$. When China can learn from U.S. exports, the U.S. lead is eroded at rate*

$$a^{open} = e_C + \iota^S,$$

while under an export control the erosion rate is

$$a^{ban} = e_C + \epsilon, \qquad 0 < \epsilon \ll \iota^S.$$

If r is the effective discount rate, the innovation prize from becoming a leader is

$$\Delta^{open} = \frac{\pi_L - \pi_N}{r + a^{open}}, \qquad \Delta^{ban} = \frac{\pi_L - \pi_N}{r + a^{ban}}. \tag{A.250}$$

Hence

$$\Delta^{ban} > \Delta^{open}, \qquad \frac{\partial \Delta}{\partial \iota^S} < 0. \tag{A.251}$$

If market size and R&D costs are otherwise unchanged, the export control raises U.S. semiconductor innovation by

$$\frac{e^{ban}}{e^{open}} = \left(\frac{r + a^{open}}{r + a^{ban}} \right)^{\frac{1}{\gamma - 1}} > 1. \tag{A.252}$$

With a simultaneous market-size loss, U.S. semiconductor innovation rises if and only if

$$\frac{E_U^{S,ban}}{E_U^{S,open}} > \frac{r + a^{ban}}{r + a^{open}}, \tag{A.253}$$

assuming $P_U Q_U^S$, λ_U^S, and κ_U^S are unchanged.

Proof When the firm is a leader, it earns the profit advantage $\pi_L - \pi_N$ until the lead is erased. The lead duration is exponentially distributed with hazard a. Therefore the present value of the leadership advantage is

$$\Delta(a) = \int_0^\infty e^{-(r+a)t}(\pi_L - \pi_N)\,\mathrm{d}t = \frac{\pi_L - \pi_N}{r + a}.$$

Since

$$\frac{\partial \Delta(a)}{\partial a} = -\frac{\pi_L - \pi_N}{(r+a)^2} < 0,$$

and $a^{ban} < a^{open}$, the export control raises the leadership prize. The innovation ratio (A.252) follows from the innovation FOC. When market size also changes, the innovation ratio is

$$\frac{e^{ban}}{e^{open}} = \left[\frac{E_U^{S,ban}}{E_U^{S,open}} \frac{\Delta^{ban}}{\Delta^{open}}\right]^{\frac{1}{\gamma-1}},$$

which is greater than one exactly when (A.253) holds. □

Proposition A.6 (Three-state semiconductor gap distribution) *Consider the truncated state space $m \in \{-1, 0, 1\}$. Let*

$$a_U^- \equiv e_U(-1) + \iota_U^S, \qquad a_C^+ \equiv e_C(1) + \iota_C^S,$$

be the rates at which the laggard catches up from -1 and 1, respectively. Let $e_U^0 \equiv e_U(0)$ and $e_C^0 \equiv e_C(0)$. The stationary distribution is

$$\mu_{-1} = \frac{e_C^0/a_U^-}{1 + e_C^0/a_U^- + e_U^0/a_C^+}, \tag{A.254}$$

$$\mu_0 = \frac{1}{1 + e_C^0/a_U^- + e_U^0/a_C^+}, \tag{A.255}$$

$$\mu_1 = \frac{e_U^0/a_C^+}{1 + e_C^0/a_U^- + e_U^0/a_C^+}. \tag{A.256}$$

The U.S. semiconductor technology advantage

$$A^S \equiv \sum_m m\mu_m = \mu_1 - \mu_{-1}$$

is decreasing in a_C^+. *Therefore, an export control that reduces China's catch-up hazard from* $e_C(1) + \iota^S$ *to* $e_C(1) + \epsilon$ *raises the U.S. semiconductor technology advantage, holding innovation rates fixed.*

Proof The stationary flow equations are

$$\mu_{-1}a_U^- = \mu_0 e_C^0, \qquad \mu_1 a_C^+ = \mu_0 e_U^0, \qquad \mu_{-1} + \mu_0 + \mu_1 = 1.$$

Solving these three equations gives (A.254)– (A.256). Let

$$A \equiv \frac{e_C^0}{a_U^-}, \qquad B \equiv \frac{e_U^0}{a_C^+}.$$

Then

$$A^S = \frac{B - A}{1 + A + B}.$$

Since

$$\frac{\partial A^S}{\partial B} = \frac{1 + 2A}{(1 + A + B)^2} > 0, \qquad \frac{\partial B}{\partial a_C^+} = -\frac{e_U^0}{(a_C^+)^2} < 0,$$

we have $\partial A^S / \partial a_C^+ < 0$. Lowering China's catch-up hazard therefore raises the U.S. semiconductor technology advantage. □

Proposition A.7 (A larger semiconductor technology advantage need not raise growth) *In the three-state environment of Proposition A.6, suppose leader innovation at* $m = 1$ *and* $m = -1$ *can raise the global frontier at rates* e_U^L *and* e_C^L, *while either country can raise the frontier from* $m = 0$. *Then*

$$g^S = \log \Lambda \left[\mu_1 e_U^L + \mu_0(e_U^0 + e_C^0) + \mu_{-1} e_C^L\right]. \tag{A.257}$$

Let $A = e_C^0/a_U^-$ *and* $B = e_U^0/a_C^+$. *A reduction in* a_C^+ *raises* B. *Holding innovation rates fixed, this raises semiconductor growth if and only if*

$$e_U^L > \frac{e_U^0 + e_C^0 + A e_C^L}{1 + A}. \tag{A.258}$$

If leader innovation is weak at high U.S. technology gaps, then an export control can increase the U.S. semiconductor technology advantage while reducing long-run semiconductor growth.

Proof Using $\mu_0 = 1/(1+A+B)$, $\mu_{-1} = A/(1+A+B)$, and $\mu_1 = B/(1+A+B)$, equation (A.257) can be written as

$$\frac{g^S}{\log \Lambda} = \frac{Be_U^L + (e_U^0 + e_C^0) + Ae_C^L}{1+A+B}.$$

Differentiating with respect to B gives

$$\frac{\partial}{\partial B}\left(\frac{g^S}{\log \Lambda}\right) = \frac{(1+A)e_U^L - (e_U^0 + e_C^0) - Ae_C^L}{(1+A+B)^2}.$$

Since a reduction in a_C^+ raises B, growth rises if and only if the numerator is positive, which is exactly (A.258). □

A.3.2 Effects on Semiconductor Price and Downstream Growth

This section shows that U.S. semiconductor control could raise China's semiconductor price, which slows down China's downstream growth.

Proposition A.8 (Downstream price channel from semiconductor trade) *Holding v_c^d, z_c, λ_c^d, and κ_c fixed, a change in the semiconductor aggregate price changes downstream productivity growth according to*

$$\frac{\partial g_c^d}{\partial \log P_c^S} = -\frac{\alpha}{1-\alpha}\lambda_c^d u_c^\alpha < 0, \tag{A.259}$$

where

$$g_c^d \equiv \frac{\dot{z}_c}{z_c} = \iota_c\left(\frac{\bar{z}}{z_c} - 1\right) + \lambda_c^d u_c^\alpha.$$

Thus semiconductor trade barriers that raise P_c^S reduce downstream growth, while reallocations that lower P_c^S raise downstream growth.

Proof By FOC of downstream innovation,

$$\frac{\partial \log u_c}{\partial \log P_c^S} = -\frac{1}{1-\alpha}.$$

The private downstream innovation component is $\lambda_c^d u_c^\alpha$. Hence

$$\frac{\partial}{\partial \log P_c^S}\left(\lambda_c^d u_c^\alpha\right) = \alpha\lambda_c^d u_c^\alpha \frac{\partial \log u_c}{\partial \log P_c^S} = -\frac{\alpha}{1-\alpha}\lambda_c^d u_c^\alpha.$$

□

A.3.3 Short-run Effects of U.S. Semiconductor Controls

Proposition A.9 (Static price impact of an export control) *Fix semiconductor prices and markups for a controlled type ω. Suppose a set of origins $\mathcal{B}_{\omega d}$ is removed from destination d's allowed supplier set. Let*

$$b_{\omega d} \equiv \sum_{o \in \mathcal{B}_{\omega d}} s_{od}^{S,0}(\omega)$$

be the pre-control expenditure share of the banned origins. Then the partial-equilibrium price increase for type ω is (holding supplier prices and markups fixed)

$$\frac{P_d^{S,1}(\omega)}{P_d^{S,0}(\omega)} = (1 - b_{\omega d})^{-\frac{1}{\sigma^S - 1}}. \tag{A.260}$$

In particular, a U.S. export ban to China has a larger direct effect on China's semiconductor price when the banned U.S. varieties have high initial shares $s_{UC}^{S,0}(m)$, which occurs when the U.S. semiconductor technology gap m is large.

Proof Let

$$X_{\omega d}^0 \equiv \sum_o \chi_{\omega o d}^0 [d_{od}^S p_{od}^S(\omega)]^{1-\sigma^S}.$$

After banning the origins in $\mathcal{B}_{\omega d}$, the CES sum is

$$X_{\omega d}^1 = (1 - b_{\omega d}) X_{\omega d}^0,$$

because $b_{\omega d}$ is the pre-control share of the removed terms in the CES sum. Since $P_d^S(\omega) = X_{\omega d}^{1/(1-\sigma^S)}$,

$$\frac{P_d^{S,1}(\omega)}{P_d^{S,0}(\omega)} = \left(\frac{X_{\omega d}^1}{X_{\omega d}^0}\right)^{\frac{1}{1-\sigma^S}} = (1 - b_{\omega d})^{-\frac{1}{\sigma^S - 1}}.$$

The final statement follows from Proposition A.1, which implies $s_{UC}^S(m)$ is increasing in the U.S. gap m, conditional on wages, trade costs, and market access. □

Proposition A.10 (Short-run semiconductor market-size condition) *Consider a U.S. export control that eliminates controlled semiconductor revenue from China but lowers the U.S. semiconductor price by $\widehat{P}_U^S < 0$ through wage and market-clearing adjustments. Holding z_U, v_U^d, and R&D costs fixed, U.S. domestic semiconductor expenditure changes by*

$$\widehat{E}_U^S = -\frac{\alpha}{1 - \alpha} \widehat{P}_U^S. \tag{A.261}$$

Let ω_U^{for} be the pre-control share of U.S. semiconductor-producer revenue coming from controlled exports to China, and let $\omega_U^{dom} = 1 - \omega_U^{for}$ be the domestic revenue share. A first-order sufficient condition for the export control to raise U.S. semiconductor market size is

$$\omega_U^{dom} \frac{\alpha}{1-\alpha}(-\widehat{P}_U^S) > \omega_U^{for}. \tag{A.262}$$

When (A.262) fails, a U.S. semiconductor innovation boom can still occur if the escape-competition term $\widehat{\Delta v}_U^S(m)$ is sufficiently positive.

Proof The partial change in domestic semiconductor expenditure is

$$\widehat{E}_U^S = \widehat{P}_U^S + \widehat{Y}_U^S = \widehat{P}_U^S - \frac{1}{1-\alpha}\widehat{P}_U^S = -\frac{\alpha}{1-\alpha}\widehat{P}_U^S.$$

Let total pre-control U.S. semiconductor-producer revenue be normalized to one. The export control removes ω_U^{for} at first order. The domestic part, with share ω_U^{dom}, changes by $\omega_U^{dom}[-\alpha\widehat{P}_U^S/(1-\alpha)]$. The total first-order market-size effect is positive exactly when (A.262) holds. □

B Empirical Results Appendix

B.1 Semiconductor Sectors and Products

Table B.1: **Semiconductor Sectors (NAICS 2022)**

Code	Name
333242	Semiconductor Machinery Manufacturing
333994	Industrial Process Furnace and Oven Manufacturing
334412	Bare Printed Circuit Board Manufacturing
334413	Semiconductor and Related Device Manufacturing
334416	Capacitor, Resistor, Coil, Transformer, and Other Inductor Manufacturing
334418	Printed Circuit Assembly (Electronic Assembly) Manufacturing
334419	Other Electronic Component Manufacturing
334513	Instruments and Related Products Manufacturing for Measuring, Displaying, and Controlling Industrial Process Variables
334515	Instrument Manufacturing for Measuring and Testing Electricity and Electrical Signals
335999	All Other Miscellaneous Electrical Equipment and Component Manufacturing

Table B.2: **Semiconductor Sectors (BEA 2017)**

Code	Name
333242	Semiconductor machinery manufacturing
333994	Industrial process furnace and oven manufacturing
33441A	Other electronic component manufacturing
334413	Semiconductor and related device manufacturing
334418	Printed circuit assembly (electronic assembly) manufacturing
334513	Industrial process variable instruments manufacturing
334515	Electricity and signal testing instruments manufacturing
335999	All other miscellaneous electrical equipment and component manufacturing

Table B.3: **Semiconductor Products (HS 2022)**

Code	Name
848610	Machines for the manufacture of boules or wafers
848620	Machines and apparatus for the manufacture of semiconductor devices or of electronic integrated circuits
848640	Machines and apparatus for manufacturing/repairing masks and reticles, assembling semiconductor devices, or for automated handling, lifting, loading/unloading of semiconductor products
848690	Parts and accessories
854140	Photosensitive semiconductor devices, solar cells, LED
854141	Light-emitting diodes (LED)
854142	Photovoltaic cells not assembled in modules or made up into panels
854143	Photovoltaic cells assembled in modules or made up into panels
854149	Other diodes: Unmounted chips, dice and wafers; Transistors; Optical coupled isolators; Other semiconductor devices
854150	Semiconductor devices
854151	Semiconductor-based transducers
854159	Other: such as Unmounted chips, dice and wafers
854190	Parts of mounted piezo-electric crystals and semiconductor devices
854211	Monolithic integrated circuits, digital
854219	Monolithic integrated circuits
854220	Hybrid integrated circuits
854231	Processors and controllers, whether or not combined with memories, converters, logic circuits, amplifiers, clock and timing circuits, or other circuits, Controllers (including microcontrollers)
854232	Memories: Dynamic read-write random access
854290	Parts of electronic integrated circuits and microassemblies
903082	For measuring or checking semiconductor wafers or devices (including integrated circuits)

B.2 Identifying Semiconductor Patents

Table B.4: Keyword filter for identifying semiconductor-related IPC codes.

Category	**Keywords**
Core semiconductor terms	*semiconductor, semiconductors, semiconducting*
Device types	*transistor, transistors, diode, diodes, thyristor, mosfet, cmos, bjt, fet, jfet, igbt, field-effect transistor, bipolar transistor*
Integrated circuits	*integrated circuit, integrated circuits, microelectronic, microprocessor, microcontroller, microchip, chip, chips, ic, vlsi, ulsi, fpga, asic, soc, system on chip*
Memory devices	*memory device, memory devices, flash memory, flash, dram, sram, rom, eprom, eeprom, non-volatile memory, volatile memory*
Optoelectronics	*led, light-emitting diode, laser diode, photodiode, photovoltaic, solar cell, solar cells, photodetector, phototransistor*

(continued on next page)

Table B.4 (continued)

Category	Keywords
Manufacturing processes	*wafer, wafers, silicon wafer, substrate, lithography, photolithography, electron beam lithography, etching, plasma etching, dry etching, wet etching, ion implantation, doping, diffusion, epitaxial, epitaxy, epitaxial growth, chemical vapor deposition, cvd, pvd, atomic layer deposition, ald, sputtering, evaporation*
Materials	*silicon, gallium arsenide, gaas, gan, sic, gallium nitride, silicon carbide, germanium, indium gallium arsenide, ingaas, crystalline, polycrystalline, amorphous*
Packaging and assembly	*packaging, encapsulation, wire bonding, flip chip, ball grid array, bga, chip scale package, csp*
Testing and characterization	*testing, characterization, measurement, probe, probing, burn-in, reliability testing, electrical testing*
Applications	*sensor, sensors, image sensor, pressure sensor, temperature sensor, accelerometer, gyroscope, mems, microelectromechanical, power semiconductor, power device, rf semiconductor, microwave semiconductor*
AI and computing	*neural network, artificial intelligence, ai chip, machine learning, deep learning, neuromorphic, quantum computing*
Advanced technologies	*nanotechnology, nanoelectronics, carbon nanotube, graphene, quantum dot, quantum well, superlattice, heterostructure*

Notes: An IPC entry is flagged as semiconductor-related if its English title or description contains any keyword listed above (case-insensitive substring match), or if its main group falls within one of the core semiconductor classifications H01L, H10B, H10H, H10K, H10N, or G11C. Keywords are applied to the official IPC English title list (`EN_ipc_title_list_20250101`).

B.3 The Top Semiconductor Innovation Economies and the U.S. Allies

Table B.5 reports the top owner economies by the number of semiconductor patent families in ORBIS IP.

B.4 Target Moments Construction

Bond holdings. $\bar{B}_U$ pins down the steady-state *trade* balance, financed by net investment income on the bond position (read as a stock, $\bar{B}_U$ is the net foreign asset position itself). We think of this as a long-term structural imbalance outside the model's scope, and thus we target the long-run

Table B.5: Owner economies by semiconductor patent families.

Owner	Families	Share (%)	Cum. (%)	Records (%)
JP	319,713	28.9	28.9	32.3
CN	270,912	24.5	53.4	17.2
KR	165,347	15.0	68.4	13.6
US	143,097	12.9	81.3	16.5
TW	100,791	9.1	90.5	8.6
DE	32,835	3.0	93.4	3.8
FR	12,675	1.1	94.6	1.7
NL	9,855	0.9	95.5	1.2
RU	6,376	0.58	96.0	0.36

Notes: Unique patent families by owner country. "Share" and "Cum." are of all semiconductor families in the dataset. "Records" counts patent records rather than families. Both measures give the same top eight. The last row is the first economy outside the bloc.

1981–2020 trade balance of the U.S. and its allies combined: -0.57%.

The semiconductor sector size. To get a measure of the total size of semiconductor sector, we rely on industry documents. According to the *2021 State of the U.S. Semiconductor Industry* (SIA report hereafter),[17] the world semiconductor sales in 2020 is $440.4 billion. Importantly, this is the worldwide sales of semiconductor *devices* — integrated circuits plus optoelectronics, sensors and discretes — measured where a semiconductor maker bills its customer. This is not one segment of the chain: it is the last transaction inside the chain, the point at which the buyer is an electronics or system firm rather than another stage of chip production. Every upstream stage is therefore already embodied in it. Silicon wafers and chemicals, EDA licences and IP cores, foundry wafer starts, assembly and test are all intermediate purchases whose cost sits inside the device price, so adding their revenues would double count. This is also what makes the number the right one for the model rather than merely the available one.

The SIA report documents the U.S. and its allies bloc account for 87% of the total semiconductor value chain.[18] The GDP at market US$ for the U.S. and its allies bloc is 36.3 trillion, and thus, we target 1.06% for the U.S. semiconductor output share of total output.[19]

[17] The Semiconductor Industry Association (SIA) is considered a premier, highly authoritative trade association and the leading voice for the semiconductor industry in the United States. The report can be accessed here: https://www.semiconductors.org/wp-content/uploads/2021/09/2021-SIA-State-of-the-Industry-Report.pdf

[18] The U.S., Taiwan, South Korea, Japan, and Europe accounts for 38%, 9%, 16%, 14%, and 10%, respectively, which sums up to 87%. China accounts for 9% and the rest accounts for 4%.

[19] $0.4404 \times 87\%/36.3 = 1.06\%$.

The size and trade of downstream sectors. The downstream innovation efficiencies set the *level* of the downstream technology stock, and therefore relative income per head. At the 2020 calibration year China's GDP per capita is 0.32 of the bloc's at PPP. The ratio of L_C/L_U pins down the relative size of the two economies. With the normalization of semiconductor labor, they also jointly pin down the size of semiconductor sector as a share of the total economy. Using PWT 11.0, the real GDP (PPP) ratio of the U.S. and its allies to China is 1.58.[20]

To discipline the downstream trade cost in the model, we target the domestic expenditure share, which is one minus the import divided by total final absorption. Thus, non-tradable output is also taken into account, since our single downstream good covers the whole economy rather than a tradable sector. Using goods trade flows from BACI (v202401b) and services from WDI, the domestic expenditure share is 85% for the U.S. and its allies, and 83% for China.

The semiconductor share of innovation input. In our model, the downstream productivity evolves as $\dot{z}_c = \lambda_c^d \left(Y_c^S\right)^\alpha z_c^{1-\alpha}$. Using $u_c \equiv Y_c^S/z_c$ and $v_c \equiv \partial V_c/\partial z_c$ (the marginal value of the productivity stock), the downstream firm's first-order condition for u_c is $(1-\kappa_c)P_c^S = \alpha\, v_c \lambda_c^d u_c^{\alpha-1}$. Multiplying through by $u_c z_c$ and and noting that $\lambda_c^d u_c^\alpha z_c$ is exactly the own-innovation term of $\dot{z}_c$, it turns into a statement about money:

$$\underbrace{(1-\kappa_c)P_c^S Y_c^S}_{\text{semiconductor bill}} \;=\; \alpha \qquad \underbrace{v_c\, \lambda_c^d u_c^\alpha z_c}_{\text{value of the productivity gain it buys}} \qquad ,$$

i.e., α is the semiconductor bill divided by the value of the innovation that bill produces. Empirically, we don't observe that value of innovation, and we use the total innovation (R&D) expenditure as the proxy.[21] On the other hand, the semiconductor bill is not value-added but the consumption. The SIA report again documents the U.S. and its allies bloc account for 54% of world semiconductor consumption, and thus the implied α is about 0.2.[22]

Productivity gap. The semiconductor productivity step λ is the engine of long-run growth in the model, so its moment is an aggregate growth rate. More specifically, we target the long-run TFP growth in the data,[23] and adjust λ to match it with the model's implied downstream productivity

[20] We have not yet adjust L_C/L_U to match this moment yet.

[21] The U.S. total R&D expenditure is from NSF NCSES, *National Patterns of R&D Resources* (NSF 26-313), Table 1, columns "Total R&D, current $billions" and "R&D/GDP total". Every other economy uses WDI data series GB.XPD.RSDV.GD.ZS (R&D, % of GDP) times that economy's GDP.

[22] The total innovation (R&D) expenditure for the U.S. and its allies in 2020 is $1,204 billion. Thus, $\alpha = 440.4 \times 54\%/1,204 \approx 19.7\%$.

[23] We use rtfpna in TFP 11.0 for all U.S. and its allies. from 1955–2023. For each country we take the annual log change of the series; the bloc growth rate in year t is the real-GDP weighted mean across members reporting that year, and

growth, g.

The US-China semiconductor technology gap. Although all internal parameters are jointly estimated, semiconductor innovation efficiency and knowledge spillover parameters $(\lambda_U^s, \lambda_C^s, \iota^S)$ are closely related to the semiconductor technology gaps. In the model, two economies' relative semiconductor technology are captured by a distribution of technology gap, instead of two scalars as for the downstream sectors. The whole distribution matters for the (aggregate) innovation incentives for two economies' semiconductor firms, as well as their innovation response to policies like export controls. Specifically, we use patent data to measure the distribution of technology gaps of semiconductor intermediates across across the two economies, and we estimate the model to reproduce this pattern by calibrating $(\lambda_U^S, \lambda_C^S, \iota^S)$. The distribution of over technology classes, and we use IPC 4-digit as our baseline granularity level, indexed by i.[24] For technology class i and year t, define

$$G_{it} = \log\left(\frac{Q_{\text{US+ally},it}}{Q_{\text{CN},it}}\right),$$

where $Q_{c,it}$ is total number of patent families filed in year t in class i by economy c. $G_i > 0$ means the US bloc leads class i.

In the model, the gap is counted in discrete quality rungs, each rung one multiplicative quality step λ — i.e. a step of $\ln\lambda$ in logs. A class's gap is therefore $G_i/\ln\lambda$ rungs, and its integer rung is

$$m_{it} \;=\; \text{round}\big(G_{it}/\ln\lambda\big), \qquad m > 0:\ \text{US + ally ahead.}$$

Note that λ is endogenous in the full calibration (pinned down by the calibrated growth rate). The data distribution $\mu_{\text{data}}(m)$ is thus the forward-citation weighted share of world families whose class lands on rung m, where the weight $w_{it} = \text{world_fwcit}_{it}$ (total normalized forward citations for all patent families in class i filed in year t, and thus a high-impact patent class counts for more).[25]

we average over the window.

[24] H01L is a special semiconductor class that requires further treatment. Every non-H01L technology remains at IPC-4, such as `H02M` or `G11C`. H01L is the semiconductor-devices-and-integrated-circuits subclass. If we treat all H01L semiconductor patents as one data point, the distribution is dominated by this one subclass: H01L carried 68% percent of all world families. Thus, we split H01L to see within-H01L heterogeneity rather than allowing one huge subclass to determine the shape of the density. We use full IPC subgroups inside H01L. For example, `H01L21/027` remains a separate technology class and in our model, a separate semiconductor intermediary.

[25] When the empirical m falls below the minimum or above the maximum of m in the model, those values are clamped to the model's minimum and max limits.

B.5 Information Technology Agreement and Semiconductor Tariffs

The Information Technology Agreement (ITA) is a plurilateral WTO agreement under which participating economies commit to bind import duties at zero on specified information-technology products. The agreement was concluded in December 1996 and implemented on a MFN basis. Accordingly, a participant grants duty-free treatment to covered imports from all WTO members, rather than only to imports from other ITA participants.[26]

The original declaration specified approximately 200 products, including key semiconductor materials and devices under HS headings 8541 and 8542.[27] The 1996 agreement default schedule required equal tariffs reductions by 1 July 1997, 1 January 1998, and 1 January 1999, followed by complete elimination on 1 January 2000. Alternative staging was permitted for a limited number of products and participants. Participation was staggered, generating additional variation in the timing of tariff reductions. For example, twenty-three participant entities joined in 1997, followed by later cohorts associated with WTO accessions or separately negotiated schedules, including China, which began participating on 24 April 2003.

B.6 Tariff Regression: Extra Results

We report extra results on how a downstream sector's innovation and other performances are affected by its semiconductor tariff exposure in Figures B.1 and B.2.

B.7 Semiconductor International Spillovers

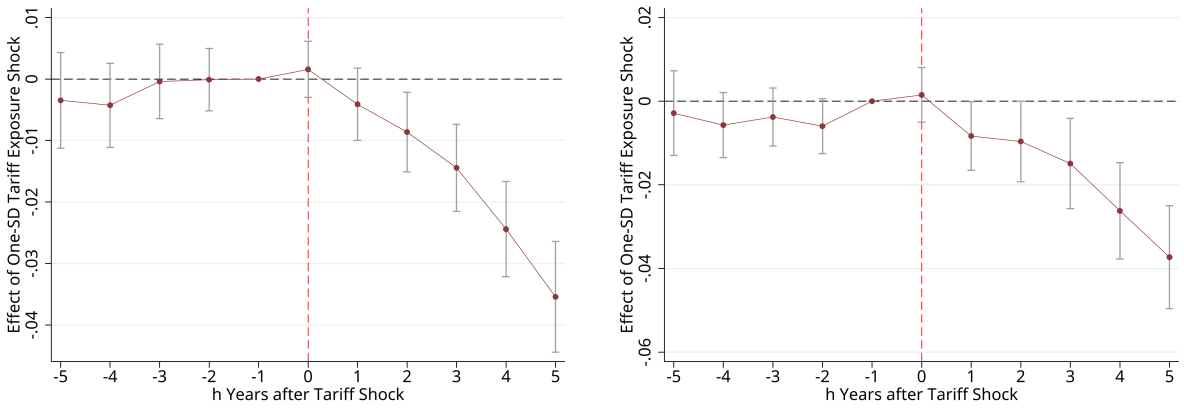
We examine semiconductor innovation spillovers from advanced to developing economies using the following specification:

$$\begin{aligned}\Delta_h y_{s,d,t} &= \beta_h \Delta x^{\text{adv}}_{s,d,t} \\ &\quad + \mathbf{1}_{\{h\geq 0\}} \sum_{l=1}^{3} \rho^l_h \Delta y_{s,d,t-l} + \sum_{l=1}^{3} \theta^l_h \Delta x_{s,d,t-l} + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t+h}, \\ \text{where } x^{\text{adv}}_{s,d,t-l} &\equiv \sum_{o\in \text{ Advanced}} \frac{\text{Citation}^{\text{Semi}}_{s,d,o,t_0}}{\text{Citation}_{s,d,t_0}} \log\left(1+\text{Patents}^{\text{Semi}}_{o,t}\right).\end{aligned} \tag{B.1}$$

[26] As of 9 June 2026, the ITA had 56 participant entities covering 84 WTO members and approximately 97 percent of world trade in information-technology products (World Trade Organization, 1996, 2026a,b).

[27] The 2015 ITA Expansion added a separate list of 201 products.

Figure B.1: Semiconductor Tariff Reduction Increases Downstream Innovation: Total Forward Citations



(a) OLS (b) IV

Notes: The outcome variable is the total forward citations. Panel (a) reports the one-standard-deviation effects estimated from Equation (2.2) in OLS. Panel (b) reports the corresponding one-standard-deviation IV estimate using (2.4). One SD refers to the exposure-weighted semiconductor tariff shock and is held fixed across outcomes and horizons. Points represent coefficient estimates, and error bars indicate 95% confidence intervals.

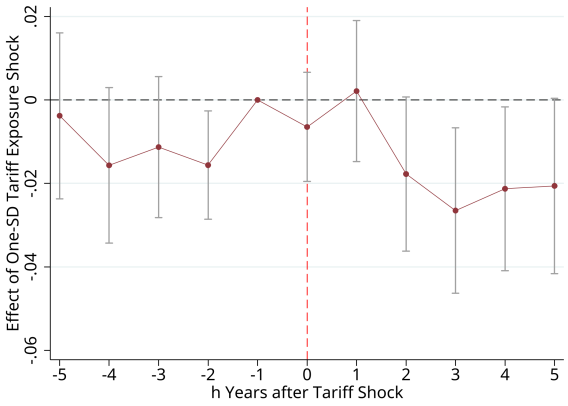
Here, $y_{s,d,t} = \log\left(1 + Patents_{s,d,t}^{Semi}\right)$, and d is a developing destination economy. Figure B.3 reports the estimation results.

B.8 Firm-level Estimation

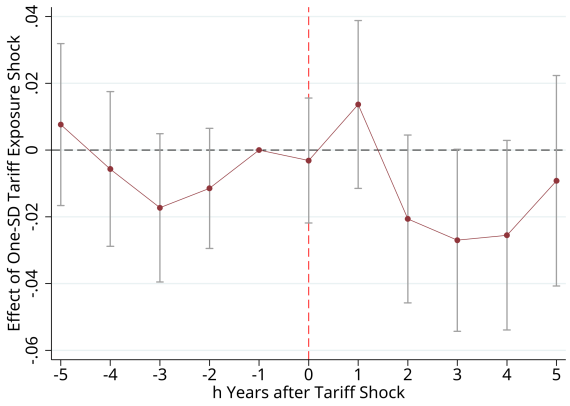
This section establishes how upstream semiconductor patent innovations affect downstream innovation at the firm level, which has several advantages over the baseline sectoral analysis. First, potential omitted factors at the country-year or sector-year level can be absorbed by fixed effects. Second, we can explore variations from firms citing different combination of semiconductor functions, and the measure of high- and low-end patents within each function. We interpret this as suggestive evidence that high-end semiconductor patent or technologies matter more for downstream innovations, and motivate our quantitative exercise that imposes export sanctions only for U.S. leading semiconductor varieties.

A patent classification and its technology sophistication: an LLM method. We summarize the idea here, and explain the detailed construction methods in Appendix **??**. The key idea is to measure the level of technology advancement or sophistication of a semiconductor patent, so the first question is what "sophistication" means here? For example, no scalar makes a DRAM cell and a GaN power transistor comparably sophisticated: they solve different problems. Instead, we

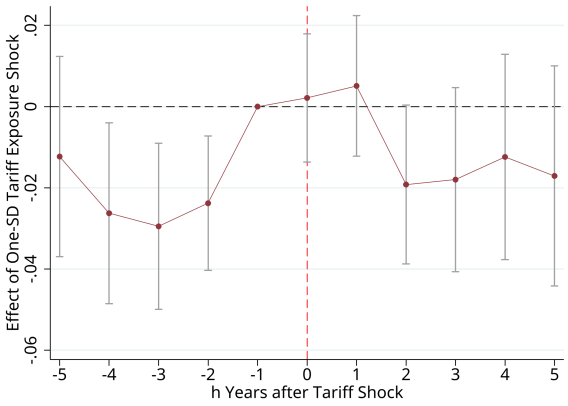
Figure B.2: Semiconductor Tariff Reduction Increases Downstream Performance



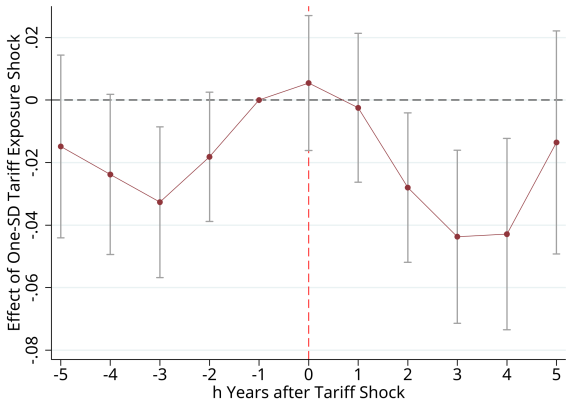
(a) Total Assets (OLS)



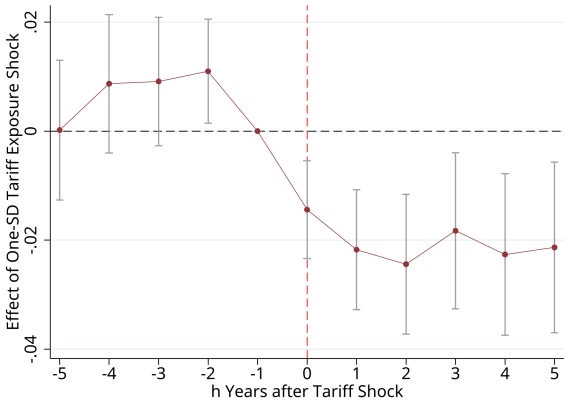
(b) Total Assets (IV)



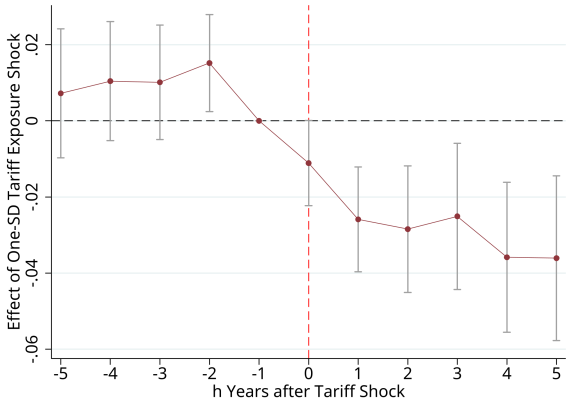
(c) Operating Revenue (OLS)



(d) Operating Revenue (IV)



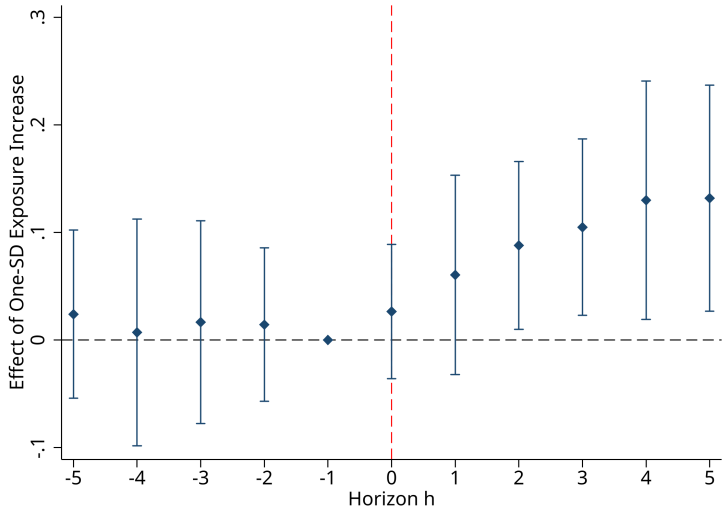
(e) Employees (OLS)



(f) Employees (IV)

Notes: This figure reports the one-standard-deviation effects estimated from Equation (2.2) in OLS, and IV estimate using (2.4). One SD refers to the exposure-weighted semiconductor tariff shock and is held fixed across outcomes and horizons. Points represent coefficient estimates, and error bars indicate 95% confidence intervals.

Figure B.3: Semiconductor Innovation Spillover from Advanced to Developing Economies



Notes: This figure reports the one-standard-deviation effects estimated from Equation (B.1) in OLS. Points represent coefficient estimates, and error bars indicate 95% confidence intervals.

want to locate each invention on its technology's roadmap. To do so, each patent is placed on three hierarchical levels: (L1) family, (L2) function, (L3) generation. Each generation is assigned one of the four tier levels: leading edge, advanced, mainstream, and legacy. We define a patent to be high-end if it is labelled as leading edge through our classification pipeline.

A *function* is the finest level at which a "frontier roadmap" can be drawn. Within a *function* — one job a device does — technology advances along a ladder of successive approaches that achieve it. The *generation* places the invention on that roadmap. For example, (function) transistor_structure runs like (generations) planar bulk CMOS → strained-Si → high-k metal gate → FinFET → GAA; (function) lithography runs like (generations) ArF → immersion → EUV. In other words, a generation is the rung a patent sits on, i.e., a specific technology/approach to realize the function, and with industrial knowledge, we can know *how advanced* the approach is. Importantly, a rung's standing, which we call tier, is *era-dependent*: each is the leading edge only within a calendar window (FinFET is the frontier ≈2012, mainstream by ≈2022), so "how advanced" is meaningful only relative to the patent filing year. The *family* sits above as the coarse domain with closely related functions, supplying a fallback tier where no roadmap exists.

A natural question is why we don't use the existing IPC classification at some level and rank patents to a tier. In other words, an IPC code might already be doing the same job as a function defined above. The answer is that IPC partitions are not designed to reflect a technological roadmap: coarse cells pool unrelated frontiers, fine cells cut a single frontier into pieces, and no depth in between escapes both. Thus, we use LLM with industrial knowledge to conduct text analysis, gives

us both a semiconductor patent classification system, and the tier for each patent.

Firm-level exposure to semiconductor functions. Denote $N_{f,t}$ to be the number of patents classified in function f and filed year t, and denote $N^{\text{lead}}_{f,t}$ to be the corresponding number of leading edge tier patents. Denote $\theta_{i,f,0}$ to be the fraction of firm i's citations that land on semiconductor function f. A citation qualifies if the citing patent family is owned by i, is not itself a semiconductor family, if the citing year is between 1990–99, and cites a family filed at most ten years earlier. The fraction is with respect to all qualifying citations that a firm cite, so $\sum_f \theta_{i,f,0}$ is the firm's semiconductor dependence.

Given the above "shifts" and "shares", we define two firm level exposure measures. The first is $E^s_{i,t} = \sum_f \theta_{i,f,0} \log(1+N_{f,t})$, which captures a firm's exposure scale to its upstream semiconductor innovation. The second is $E^q_{i,t} = \sum_f \theta_{i,f,0} \left(\log(1+N^{\text{lead}}_{f,t}) - \log(1+N_{f,t})\right)$, which captures a firm's exposure composition to its upstream semiconductor innovation.

Sample. The sample included in the regressions are firms with any qualifying 1990–99 citations, with at least one of them to a semiconductor family, with at least 20 citations in total, who on average at least has one non-semiconductor family a year over 1994–2019, and under 10% of its own patents are semiconductor patents. That leaves 6,698 firms holding around 15% of 2000–19 downstream patenting, which suggests that these are established and innovation-intensive firms.

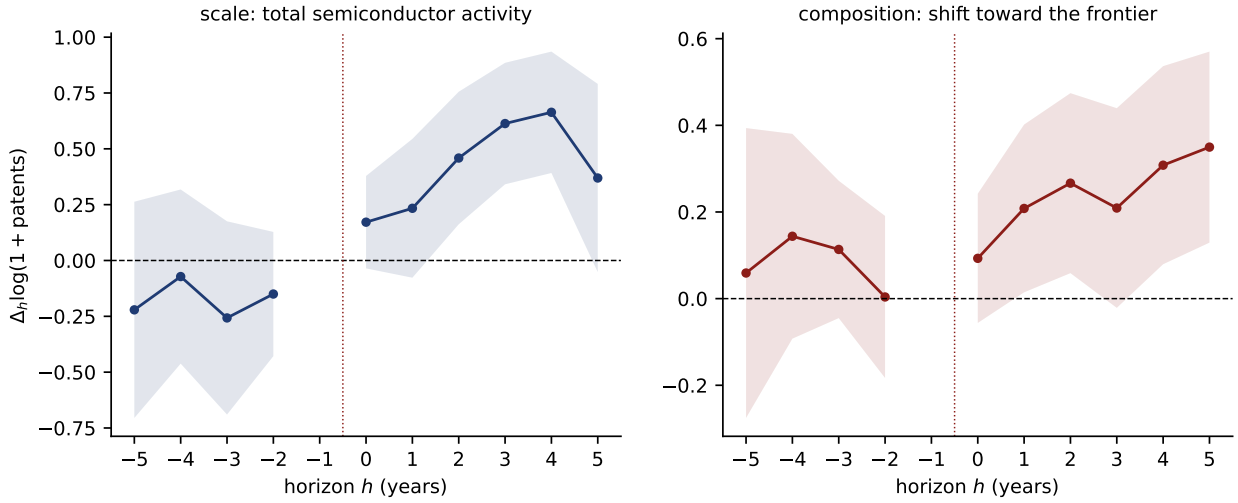
The specification. For each horizon $h = -5, \ldots, 5$ separately,

$$\begin{aligned}\Delta_h y_{i,t} = {} & \beta^s_h \, \Delta E^s_{i,t} + \beta^q_h \, \Delta E^q_{i,t} \\ & + \sum_{l=1}^{3} \left(\theta^l_h \Delta E^s_{i,t-l} + \theta^l_h \Delta E^q_{i,t-l}\right) + \underbrace{a_i + b_i t}_{\text{firm trend}} + \gamma_{d(i),t} + \gamma_{s(i),t} + \varepsilon_{i,t+h}.\end{aligned} \tag{B.2}$$

The firm intercept and trend remove the firm's average patenting rate and its secular path, so nothing is identified from big firms patenting more or from a firm's own decline. $\gamma_{d,t}$ removes anything hitting all firms of a country in a year, such as a national R&D cycle, an exchange rate, a patent-office change. $\gamma_{s,t}$ removes anything hitting a technology sector (IPC4 subclass) in a year, so a firm is compared with other firms in the same IPC class in the same year; this is what makes the estimate about semiconductor exposure rather than about being in electronics during the 2000s. The three lags of each exposure change matter because again exposures are potentially serially correlated: without them β_h mixes the response to the date-t innovation with responses to earlier ones.

Figure B.4 shows the result for outcome variable y being the firm's number of patents. The

results suggest a clear downstream patenting increase to more semiconductor innovation relevant to a firm. Moreover, holding total semiconductor innovation scale fixed, a shift of the relevant upstream semiconductor innovation for a firm toward the more leading edge technologies raises downstream patenting.



Notes: the two coefficients of equation (B.2), estimated together; bands are 95% exposure-robust intervals. The outcome lags enter at $h \geq 0$ only, so the negative horizons are estimated without them. 6,698 firms over 2000–2019; 133,960 firm-year observations at $h \leq 0$ falling to 107,168 at $h = 4$ and 100,470 at $h = 5$ as the outcome window runs out. Standard errors cluster on 95 semiconductor functions.

Figure B.4: Firm level estimations: Scale and composition.

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