Short-Run Boom, Long-Run Bust: The Dynamic Impact of U.S. Semiconductor Export Controls

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Abstract

We document novel empirical evidence demonstrating how semiconductor innovation drives downstream innovation in the U.S. and China. We then develop a two-country endogenous growth model where semiconductor firms make strategic investments and downstream firms rely on semiconductors as critical innovation inputs, positioning semiconductor innovation as the primary engine for long-run economic growth. Estimating this model, we evaluate the impact of U.S. semiconductor export controls on bilateral innovation and productivity. Our analysis yields two key findings. First, U.S. export controls generate a short-run innovation boom in domestic semiconductor and downstream sectors—driven by a stronger escape-competition motive and increased domestic supply of semiconductors, respectively—while suppressing Chinese semiconductor innovation. In the long run, however, the loss of the Chinese market causes U.S. innovation to decline across both sectors, regardless of whether the U.S. successfully widens its technological lead. Second, a positive downstream productivity shock (e.g., AI advancements) magnifies the short-run benefits and mitigates the long-run losses of these export controls on U.S. downstream innovation.

Keywords: Industrial policy, economic growth, U.S.-China technology competition, innovation.

JEL classification: F40, O10, O30, O40, O50.

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1 Introduction

The semiconductor industry is at the core of the ongoing U.S.–China technology competition. In recent years, the United States has tightened restrictions on China's access to advanced-node semiconductors, high-end manufacturing equipment, and related computing technologies, while also coordinating with allies such as Japan and the Netherlands to implement similar controls. This strategic shift was articulated by U.S. National Security Advisor Jake Sullivan at the SCSP Global Emerging Technology Summit (September 16, 2022):

> "We previously maintained a 'sliding scale' approach that said we need to stay only a couple of generations ahead. That is not the strategic environment we are in today. Given the foundational nature of certain technologies, such as advanced logic and memory chips, we must maintain as large of a lead as possible."

These policies are economically important for two reasons. First, semiconductors are dual-use technologies with both civilian and military applications, which motivates national-security-based intervention (e.g., Goldberg and Reed (2023)). Second, semiconductors are general-purpose innovation inputs that power AI, digital technologies, and productivity growth across a wide set of downstream industries (e.g., Aiyar, Chen, Ebeke, Garcia-Saltos, Gudmundsson, Ilyina, Kangur, Kunaratskul, Rodriguez, Ruta, Schulze, Soderberg, and Trevino (2023)). At the same time, the U.S.–China semiconductor race has become more competitive: as shown in Figure 1.1, the U.S.–China semiconductor technology gap has narrowed over time, based on both patent quantity and forward-citation measures.

Despite strong policy interest, the economic effects of semiconductor export controls remain insufficiently understood. Existing discussions typically emphasize either national-security gains or market-share losses for affected firms, but offer less guidance on dynamic, economy-wide innovation consequences. This distinction is crucial: export controls may have very different short-run and long-run effects through multiple channels, including strategic innovation incentives, market-size changes, input-price adjustments, and cross-country knowledge diffusion.

This paper asks: How do U.S. semiconductor export controls affect innovation, productivity growth, and welfare in the U.S. and China over time? To answer this question, we combine new

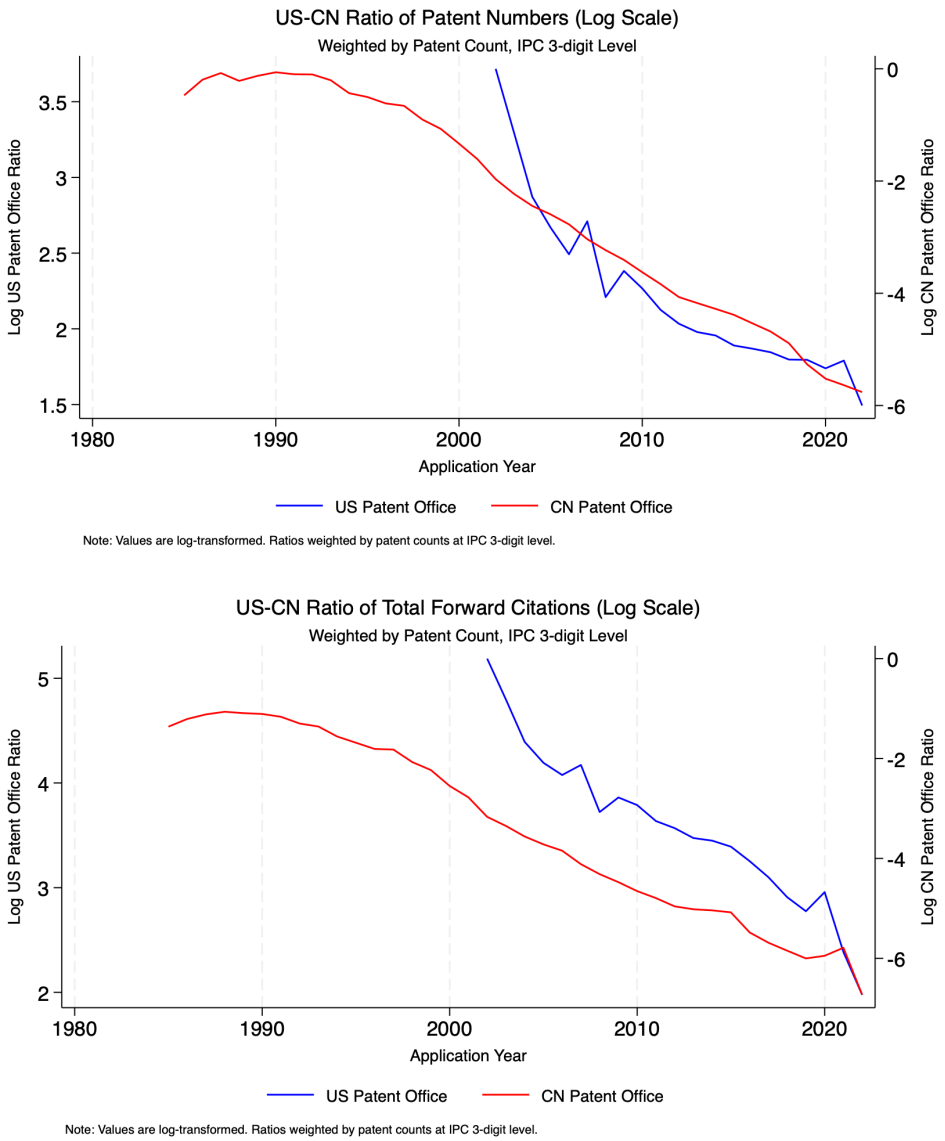


Figure 1.1: China–U.S. Semiconductor Technology Gap over Time

empirical evidence with a two-country quantitative endogenous growth model.

Our empirical analysis first documents novel facts on the semiconductor–downstream innovation linkage. Using a newly constructed global firm-level dataset that merges semiconductor firm lists across value-chain segments with ORBIS historical and intellectual-property data, we show three robust patterns. First, semiconductor innovation strongly predicts downstream innovation. Second, foreign semiconductor innovation often has larger effects than domestic semiconductor innovation, highlighting the role of international technological interdependence. Third, semiconductor import

exposure promotes downstream innovation, while semiconductor tariff exposure reduces it. These facts motivate and discipline the model's core mechanisms.

Guided by this evidence, we develop a two-country endogenous growth model with strategic semiconductor innovation and downstream innovation. In the semiconductor sector, firms compete in a step-by-step innovation environment where innovation incentives depend on endogenous markups, market shares, and bilateral technology gaps. In the downstream sector, firms use semiconductors as essential innovation inputs; hence semiconductor prices and availability directly shape downstream R&D intensity and aggregate productivity growth. The model also incorporates international trade in downstream goods and semiconductor goods, policy-contingent semiconductor trade barriers, and cross-country knowledge diffusion. This structure allows us to trace both direct effects (on semiconductor firms) and general-equilibrium propagation (to downstream innovation, wages, trade balances, and welfare).

Our quantitative strategy proceeds in three steps. First, we parameterize externally standard preference, technology, and trade cost parameters. Second, we internally estimate key innovation and diffusion parameters by matching moments from both macro data and our micro empirical estimates, including moments that capture (i) semiconductor innovation effects on downstream innovation, (ii) semiconductor import effects on downstream innovation, (iii) U.S. semiconductor trade patterns, and (iv) aggregate growth and R&D intensity. Third, we solve for transition dynamics between balanced growth paths under counterfactual export-control regimes. This transition-path approach is central: it enables us to quantify short-run gains, long-run losses, and their decomposition into market-size, input-cost, and knowledge-diffusion channels.

Our analysis yields a clear dynamic pattern: short-run boom, long-run bust. In the short run, U.S. export controls can increase domestic semiconductor and downstream innovation. The mechanism is twofold: reduced foreign sales reallocate semiconductor supply domestically (lowering local semiconductor prices for downstream innovators), and strategic competition effects can strengthen U.S. innovation incentives relative to China. In the long run, however, loss of access to the Chinese market reduces the scale of returns to U.S. semiconductor innovation, which in turn depresses downstream innovation and productivity growth. Importantly, this long-run decline can arise even when the U.S. widens its technology lead over China. We also show that a positive downstream

innovation shock (e.g., AI-related advances) amplifies short-run gains and mitigates long-run losses, underscoring that policy effects depend on the broader innovation environment.

Related Literature. This project contributes to several strands of the literature. First, we contribute a new model to the literature on trade and innovation (e.g., Eaton and Kortum (1999), Atkeson and Burstein (2010), Bustos (2011), Cai, Li, and Santacreu (2022), Sampson (2023), Bai, Jin, Lu, and Wang (2023), Cong, Kaniel, and Xiao (2023), Santacreu (2025), Chen, Fan, and Luo (2023), Liu and Ma (2023)). Industry evidence suggests that semiconductor firms make innovation decisions strategically, taking into account their technological distance from competitors. This makes step-by-step innovation models a natural framework (see, e.g., Aghion, Harris, Howitt, and Vickers (2001), Aghion, Bloom, Blundell, Griffith, and Howitt (2005), Akcigit, Ates, and Impullitti (2018), Sui (2023)): firms make innovation investments in light of competitors' strategies and relative technological distance, a behavior often termed "strategic innovation." We extend the step-by-step framework by introducing downstream innovation that uses semiconductors as innovation inputs and by showing how semiconductor firms' strategic decisions affect economy-wide innovation.

Second, we provide new empirical evidence on the links between semiconductor and downstream innovation. Prior studies on semiconductors typically focus on the industry itself, examining prices and market shares (Irwin and Klenow (1994); Aizcorbe and Kortum (2005); Miao (2023)). In contrast, we use firm-level patent and balance sheet data to document new facts, which inform the quantitative evaluation of different policy scenarios.

Third, we contribute to the burgeoning literature on sanctions, conflicts, and political preferences in international trade (e.g., Becko and O'Connor (2024); Bonfatti and O'Rourke (2018); Broner, Martin, Meyer, and Trebesch (2023); Clayton, Maggiori, and Schreger (2023); de Souza, Hu, Li, and Mei (2024); Kleinman, Liu, and Redding (2020); Morelli and Sonno (2017); Thoenig (2024)). Unlike previous studies that focus on policies related to political relationships and national security threats posed by China's semiconductor advancement, our contribution lies in emphasizing the impact on economy-wide innovation.

Roadmap. The rest of the paper proceeds as follows. Section 2 presents data construction and empirical findings. Section 3 develops the model and clarifies mechanisms. Section 4 describes parameterization and counterfactual transition-path results. Section 5 concludes.

2 Data, Variable Construction, and Empirical Findings

The model suggests that the impact of U.S. semiconductor export controls depends on both the effectiveness of semiconductors in promoting downstream innovation, the differential effects of domestic versus foreign semiconductors, and the effects of downstream innovation on semiconductor innovation. In this section, we present data and empirical evidence to inform and calibrate the relevant parameters in the model.

2.1 Semiconductor Firms, Downstream Firms, Innovation, and Balance Sheet

We use several important industry organization member list[1] to construct a novel semiconductor firm list spanning over most important countries and segments of value chains.The combined list include 5780 firms. The key difference and advantage of our data over existing data sources, such as Goldberg et al. (2024); Miao (2023); OECD (2019), is the comprehensive coverage along the whole semiconductor value chain. The major segments in semiconductor global value chains include (1) chip design, (2) wafer fabrication, (3) assembly, packaging, and testing (APT), (4) electronic design automation (EDA) and core IP, and (5) semiconductor manufacturing equipment. Existing papers mostly use data on the fabrication stage, presumably because the overall technology level of a chip is to a large extent reflected in the fabrication stage and easier to measure (using the "node size"). Fabrication related firm data are also easier to collect as there are few fabrication firms around the globe. However, all segments above consist important value-added for the semiconductor industry, and technology progress are made along the whole chain.

As a robustness check, we use semiconductor industry and IPC codes from previous research

[1]The list sources are: (1) SEMI, (2) China Semiconductor Industry Association, (3) companiesmarketcap.com/semiconductors, (4) Semiconductor Industry Association, (5) Japan Electronics and Information Technology Industries Association, (6) Semiconductor Equipment Association of Japan, (7) Taiwan Semiconductor Industry Association, (8) Korea Semiconductor Industry Association, (9) Wikipedia: semiconductor companies.

to generate a list of semiconductor firms based on the ORBIS Historical and ORBIS Intellectual Property databases.

We then merge the semiconductor firm list with the ORBIS Historical and ORBIS Intellectual Property database using fuzzy matching algorithm, supplemented by manual verification. All non-semiconductor firms are classified as downstream firms.

This process allows us to associate each firm with its firm level sales and patent variables. Although patents may not capture all innovation activities of firms, patents represent the best available and most reliable measure of innovation. The data includes patents filed in around 40 patent offices worldwide. We focus on data from the period since 1990.

2.2 Semiconductor Output, Trade and Tariff

Semiconductor sector output data comes from ORBIS, and input-output data across industries is from the U.S. BEA. Semiconductor import data is obtained from UN Comtrade. The applied tariff data for semiconductors is from the World Bank WITS database. We merge product and industry codes (HS or NAICS codes) with the ORBIS Historical and ORBIS Intellectual Property database using NAICS codes. The matching between NAICS and HS codes is based on established algorithms.

2.3 Empirical Findings

2.3.1 Fact 1. Semiconductor Innovation Increases Downstream Innovation

For sector (identified using IPC codes) s in destination country d in year t, we estimate

$$Outcome_{s,d,t} = \beta \sum_{o} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{o,t}\right) + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t}, \tag{2.1}$$

where $Citation^{Semi}_{s,d,o,t_0}$ denotes citation by sector s in country d to semiconductor sector in country o in the initial year of the sample. $Citation_{s,d,t_0}$ denotes the total citations of sector s in country d in the initial year. $Patents^{Semi}_{o,t}$ denotes the number of granted patents filed by semiconductor

sector in country o and year t. The outcome variables include the number of granted patents, sales, estimated TFPR and so on. To study the domestic semiconductor innovation effect and the foreign semiconductor innovation effect separately, we estimate

$$\begin{aligned} Outcome_{s,d,t} =& \beta_1 \frac{Citation^{Semi}_{s,d,d,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{d,t}\right) + \beta_2 \sum_{o \neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{o,t}\right) \\ &+ \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t}, \end{aligned} \tag{2.2}$$

Columns (2) and (4) of Table 2.1 show that the foreign effect is stronger than the domestic effect. To separate the effects of high-end semiconductors and low-end semiconductors, we estimate

$$\begin{aligned} Outcome_{s,d,t} =& \beta_1 \frac{Citation^{Semi,q}_{s,d,d,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi,q}_{d,t}\right) + \beta_2 \sum_{o \neq d} \frac{Citation^{Semi,q}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi,q}_{o,t}\right) \\ &+ \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t}, q \in \{High, Low\} \end{aligned} \tag{2.3}$$

where high-end and low-end semiconductors are identified by keywords in patent abstracts. For example, high-end semiconductors typically include terms such as "advanced," "high performance," "AI," "5G," "machine learning," or "EUV" in their patent abstracts, while low-end semiconductors often feature keywords like "low-cost," "low power," "simple," "legacy," or "embedded."

Note that potential endogeneity issues are not problematic, as both the data and the model account for the possibility that downstream innovation could affect semiconductor innovation. The magnitude of this positive correlation is useful for disciplining the model.

2.3.2 Fact 2. Semiconductor Import Increases Downstream Innovation

For downstream sector (non-semiconductor sector) s from importing country d in year t, we estimate

$$Outcome_{s,d,t} = \beta \Gamma^{s,Semi} \log\left(\sum_o IMP^{Semi}_{d,o,t}\right) + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t}, \tag{2.4}$$

where $\Gamma^{s,Semi}$ represents the share of semiconductors in the total intermediate inputs required for production in a 6-digit sector s, $IMP^{Semi}_{d,o,t}$ denotes total import value of semiconductors from country o. IV for $\Gamma^{s,Semi} \log\left(\sum_o IMP^{Semi}_{d,o,t}\right)$: $\Gamma^{s,Semi} \log\left(\sum_o IMP^{Semi}_{d,o,t_0} Applied\ MFN\ Tariff^{Semi}_{d,o,t}\right)$.

Table 2.1: **Semiconductor Innovation Increase Downstream Innovation**

Dep.var	$\log(Patent\ Application_{sdt})$		$\text{asinh}(Patent\ Application_{sdt})$	
	(1)	(2)	(3)	(4)
$\sum_o \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log(Patents^{Semi}_{o,t})$	0.037***			
	(0.001)			
$\sum_o \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}(Patents^{Semi}_{o,t})$			0.034***	
			(0.001)	
$\frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{d,t}\right)$		0.020***		
		(0.002)		
$\sum_{o\neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log(Patents^{Semi}_{o,t})$		0.043***		
		(0.001)		
$\frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}\left(Patents^{Semi}_{d,t}\right)$				0.017***
				(0.002)
$\sum_{o\neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}(Patents^{Semi}_{o,t})$				0.039***
				(0.001)
Observations	115,372	115,372	115,372	115,372
Adjusted R-squared	0.833	0.834	0.840	0.836
Importing Country × Sector FE	Yes	Yes	Yes	Yes
Importing Country × Year FE	Yes	Yes	Yes	Yes
Sector × Year FE	Yes	Yes	Yes	Yes

Notes: Robust standard errors clustered at the sector level are reported in parentheses below the coefficients. Asterisks denote significance levels * < 0.1, ** < 0.05, *** < 0.01.

An alternative specification is

$$\Delta \log(Outcome_{s,d,t}) = \beta \Gamma^{s,Semi} \sum_o \frac{IMP^{Semi}_{d,o,t}}{Output^{Semi}_{d,t}} \Delta \log(IMP^{Semi}_{d,o,t}) + \gamma_{d,s}(+\gamma_{d,t} + \gamma_{s,t}) + \epsilon_{s,d,t}, \tag{2.5}$$

and the alternative IV is: $\Gamma^{s,Semi} \sum_o \frac{IMP^{Semi}_{d,o,t_0}}{Output^{Semi}_{d,t_0}} Applied\ MFN\ Tariff^{Semi}_{d,o,t}$. This specification seems to be better than regressing different outcomes directly on tariff. The previous specification only delivers significant results for downstream innovation but not for other outcomes.

Table 2.2: **Semiconductor Innovation Increase Downstream Innovation (USA: High- v.s Low-end)**

Dep.var	High-end Patent				Low-end Patent			
	log ($Patent\ Application_{sdt}$)		asinh ($Patent\ Application_{sdt}$)		log ($Patent\ Application_{sdt}$)		asinh ($Patent\ Application_{sdt}$)	
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\sum_o \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{o,t}\right)$	0.200***				0.153***			
	(0.009)				(0.005)			
$\sum_o \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}\left(Patents^{Semi}_{o,t}\right)$			0.185***				0.142***	
			(0.008)				(0.005)	
$\frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{d,t}\right)$		0.154***				0.183***		
		(0.012)				(0.009)		
$\sum_{o\neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{o,t}\right)$		0.333***				0.226***		
		(0.012)				(0.007)		
$\frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}\left(Patents^{Semi}_{d,t}\right)$				0.149***				0.175***
				(0.012)				(0.008)
$\sum_{o\neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}\left(Patents^{Semi}_{o,t}\right)$				0.304***				0.210***
				(0.011)				(0.006)
Observations	92,702	92,702	92,702	92,702	143,692	143,692	143,692	143,692
Adjusted R-squared	0.680	0.682	0.681	0.683	0.612	0.614	0.613	0.614
Importing Country × Sector FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Importing Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Sector × Year FE	No	No	No	No	No	No	No	No

Notes: Robust standard errors clustered at the sector level are reported in parentheses below the coefficients. Asterisks denote significance levels $^{*} < 0.1$, $^{**} < 0.05$, $^{***} < 0.01$.

2.3.3 Fact 3. Semiconductor Tariff Reduces Downstream Innovation

$$Outcome_{s,d,t} = \beta \Gamma^{s,Semi} \sum_o \frac{IMP^{Semi}_{d,o,t}}{Output^{Semi}_{d,t}} Tariff^{Semi}_{d,o,t} + \gamma_{d,s} + \gamma_{d,t} + \gamma_{s,t} + \epsilon_{s,d,t}, \tag{2.6}$$

where s denotes a downstream sector, d denotes importing country. $IMP^{Semi}_{d,o,t}$ denotes semiconductor import from origin country o. It is divided with country d's semiconductor output to measure the importance of import for semiconductor sector in country d. $Tariff^{Semi}_{d,o,t}$ denotes the semiconductor sector tariff that d imposes on o in year t.

$\sum_o \frac{IMP^{Semi}_{d,o,t}}{Output^{Semi}_{d,t}} Tariff^{Semi}_{d,o,t}$ measures country d's overall exposure to semiconductor tariffs. Regressor $\Gamma^{s,Semi} \sum_o \frac{IMP^{Semi}_{d,o,t}}{Output^{Semi}_{d,t}} Tariff^{Semi}_{d,o,t}$ captures how downstream sector d is exposed to these tariffs.

To create exogenous variation for downstream sector's exposure to semiconductor tariff, I follow Boehm et al. (2023) and instrument applied tariff with applied MNF tariff. The idea is as follows.

Table 2.3: **Semiconductor Innovation Increase Downstream Innovation (CHN: High- v.s Low- end)**

Dep.var	High-end Patent				Low-end Patent			
	$\log(Patent\ Application_{sdt})$		$\text{asinh}(Patent\ Application_{sdt})$		$\log(Patent\ Application_{sdt})$		$\text{asinh}(Patent\ Application_{sdt})$	
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\sum_o \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log(Patents^{Semi}_{o,t})$	0.054***				0.050***			
	(0.006)				(0.002)			
$\sum_o \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}(Patents^{Semi}_{o,t})$			0.049***				0.046***	
			(0.005)				(0.002)	
$\frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log\left(Patents^{Semi}_{d,t}\right)$		0.095***				0.051***		
		(0.007)				(0.003)		
$\sum_{o\neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \log(Patents^{Semi}_{o,t})$		0.049***				0.055***		
		(0.006)				(0.003)		
$\frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}\left(Patents^{Semi}_{d,t}\right)$				0.086***				0.047***
				(0.006)				(0.003)
$\sum_{o\neq d} \frac{Citation^{Semi}_{s,d,o,t_0}}{Citation_{s,d,t_0}} \text{asinh}(Patents^{Semi}_{o,t})$				0.044***				0.050***
				(0.005)				(0.003)
Observations	7,667	7,667	7,667	7,667	38,157	38,157	38,157	38,157
Adjusted R-squared	0.648	0.653	0.654	0.659	0.722	0.722	0.726	0.726
Importing Country × Sector FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Importing Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Sector × Year FE	No	No	No	No	No	No	No	No

Notes: Robust standard errors clustered at the sector level are reported in parentheses below the coefficients. Asterisks denote significance levels $^{*} < 0.1$, $^{**} < 0.05$, $^{***} < 0.01$.

A country adjusts product MFN tariff mostly based on domestic need and negotiation with major trade partners. Hence, if the country applies MFN tariff to a smaller trade partner, and the MFN tariff is changed, such tariff change is likely exogeneous to the country's trade relationship with the smaller trade partner. We define *Applied MFN Tariff* as follows:

$$\begin{aligned} Applied\ MFN\ Tariff^{Semi}_{d,o,t} = MFN\ Tariff^{Semi}_{d,t} &\times \mathbb{1}\{d\ applies\ MFN\ to\ o\} \\ &\times \mathbb{1}\{o\ is\ not\ d's\ top\ 5\ trade\ partners\} \end{aligned} \tag{2.7}$$

and hence the IV is $\Gamma^{s,Semi} \sum_o \frac{IMP^{Semi}_{d,o,t_0}}{Output^{Semi}_{d,t_0}} Applied\ MFN\ Tariff^{Semi}_{d,o,t}$.

I plan to make event study plots based on this specification. For now, I did not add controls, $\mathbf{X}_{s,d,t}$. Will probably add them later.

Table 2.4: **Semiconductor Imports Increases Downstream Innovation (OLS)**

Dep.var	$\log(Total\ Asset_{sdt})$	$\log(Revenue_{sdt})$	$\log(Number\ of\ Employees_{sdt})$	$\log(Number\ of\ Patents_{sdt})$	$\text{asinh}(Total\ Asset_{sdt})$	$\text{asinh}(Revenue_{sdt})$	$\text{asinh}(Number\ of\ Employees_{sdt})$	$\text{asinh}(Number\ of\ Patents_{sdt})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\Gamma^{s(i),Semi} \times \log(\sum_o IMP^{Semi}_{d,o,t})$	0.131***	0.135***	0.087***	0.024	0.208***	0.166***	0.095***	0.189***
	(0.024)	(0.030)	(0.023)	(0.018)	(0.052)	(0.055)	(0.033)	(0.038)
Observations	647,935	674,896	593,664	102,169	757,471	757,471	757,471	757,471
Adjusted R-squared	0.871	0.850	0.856	0.732	0.872	0.750	0.831	0.686
Importing Country × Sector FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Importing Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Sector × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Notes: Robust standard errors clustered at the importing country - sector level are reported in parentheses below the coefficients. Asterisks denote significance levels * < 0.1, ** < 0.05, *** < 0.01.

Table 2.5: **Semiconductor Tariff Reduces Downstream Innovation (OLS)**

Dep.var	$\log(Number\ of\ Patents_{sdt})$			$\text{asinh}(Number\ of\ Patents_{sdt})$		
	(1)	(2)	(3)	(4)	(5)	(6)
$\Gamma^{s,Semi} \sum_o \frac{IMP^{Semi}_{d,o,t}}{Output^{Semi}_{d,t}} Tariff^{Semi}_{d,o,t}$	-0.009***	-0.029***	-0.011***	-0.001***	-0.026***	-0.017***
	(0.002)	(0.003)	(0.004)	(0.0002)	(0.001)	(0.001)
Observations	110,708	108,744	108,443	806,831	809,201	808,832
Adjusted R-squared	0.585	0.122	0.438	0.547	0.107	0.391
Importing Country × Sector FE	Yes	No	No	Yes	No	No
Sector × Year FE	No	Yes	Yes	No	Yes	Yes
Importing Country × Year FE	No	No	Yes	No	No	Yes

Notes: Robust standard errors clustered at the importing country - sector level are reported in parentheses below the coefficients. Asterisks denote significance levels * < 0.1, ** < 0.05, *** < 0.01.

3 Model

The economy is in continuous time with infinite horizon and consists of two countries: the U.S. (U) and China (C), indexed by $c \in \mathbb{C}$, where $\mathbb{C} = \{U, C\}$. We focus on a stationary balanced growth path equilibrium and on the transition dynamics between balanced growth paths. The setup of the model is shown in Figure 3.1, with the details summarized as follows.

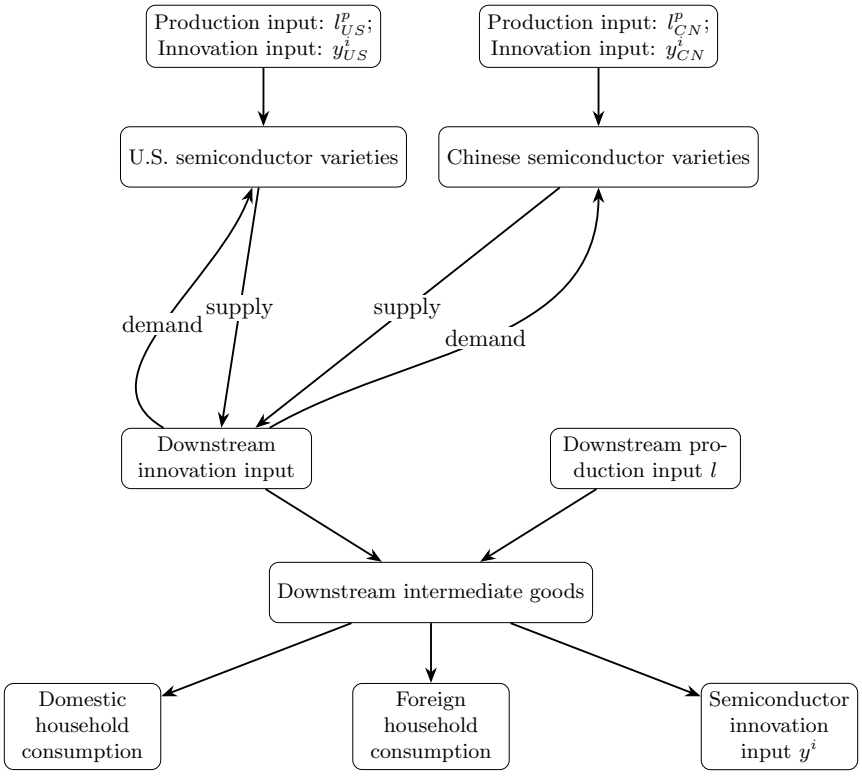


Figure 3.1: Model Setup

3.1 Model Setup

3.1.1 Representative Households

In period t, the households in each country c maximize utility:

$$\max_{C_{c,s},B_{c,s}} U_{c,t} \equiv \mathbb{E}_t \int_t^\infty \exp(-\rho(s-t)) \ln C_{c,s} ds, \tag{3.1}$$

subject to the flow budget constraint

$$P^d_{c,t} C_{c,t} + \dot{B}_{c,t} + \frac{\eta}{2}(B_{c,t} - \bar{B}_c)^2 = w_{c,t} L_c + w^{\text{semi}}_{c,t} L^{\text{semi}}_c + \Pi^{\text{all}}_{c,t} - P^d_{c,t} \text{RD}^{\text{semi}}_{c,t} - P^{SA}_{c,t} Y^{SA}_{c,t} + R_t B_{c,t} + \text{Tr}_{c,t}, \tag{3.2}$$

where ρ is the discount factor, $C_{c,t}$ is the consumption of final good, $P^d_{c,t}$ is the price of consumption goods, L_c and L^{semi}_c denote the labor supply of downstream goods and semiconductors, respectively. Labor is immobile across countries, a standard assumption in the trade literature. Two types of labor

supply are considered, as the data show that semiconductor-related workers account for a limited labor supply in the total economy and earn a different wage rate. $w_{c,t}$ and $w^{\text{semi}}_{c,t}$ denote the wage rate for each type of labor supply. $B_{c,t}$ denotes the stock of internationally traded risk-free bonds yielding an instantaneous net interest rate R_t, $\dot{B}_{c,t}$ denotes the net accumulation of these bonds, $\bar{B}_c$ denotes steady state bond holdings, $\eta > 0$ indicates quadratic adjustment cost of international portfolios to ensure unique steady state solution (cf. Schmitt-Grohé and Uribe (2003)), $\Pi^{\text{all}}_{c,t}$ denotes production profits of downstream firms and semiconductor firms, $\text{Tr}_{c,t}$ denotes quadratic adjustment cost rebated to households, $\text{RD}^{\text{semi}}_{c,t}$ denotes semiconductor innovation cost, and $P^{SA}_{c,t}Y^{SA}_{c,t}$ denotes downstream firms' expenditures on semiconductors. The utility maximization problem leads to a standard Euler equation:

$$\eta(B_{c,t} - \bar{B}_c) + \frac{\dot{P}^d_{c,t}}{P^d_{c,t}} + \frac{\dot{C}_{c,t}}{C_{c,t}} + \rho = R_t, \tag{3.3}$$

where $\frac{\dot{C}_{c,t}}{C_{c,t}}$ and $\frac{\dot{P}_{c,t}}{P_{c,t}}$ denote the growth rate of consumption and final good price.

3.1.2 Final Good Technology

A non-tradable, perfectly competitive final good $Y^d_{c,t}$ is produced using $T_{c',t}$ number of downstream goods $y_{c'c,t}$ from countries $c' \in \mathbb{C}$ according to

$$Y^d_{c,t} = \left(\sum_{c'} T_{c',t} (y_{c'c,t})^{\frac{\sigma-1}{\sigma}} \right)^{\frac{\sigma}{\sigma-1}}, \tag{3.4}$$

where $\sigma > 1$ represents the elasticity of substitution across downstream goods. The profit maximization problem of the final good producers gives the demand function:

$$y_{c'c,t} = \left(\frac{d_{c'c} p_{c'c,t}}{P^d_{c,t}}\right)^{-\sigma} Y^d_{c,t}, \tag{3.5}$$

where the final good price is given by $P^d_{c,t} = \left(\sum_{c'} T_{c',t} (d_{c'c} p_{c'c,t})^{1-\sigma}\right)^{\frac{1}{1-\sigma}}$, $p_{c'c,t}$ denotes the price of downstream goods and $d_{c'c} \geq 1$ denotes the downstream trade costs.

3.1.3 Downstream Goods Production

$T_{c,t}$ number of monopolistically competitive intermediate goods producers employ labor $l_{c,t}$ to produce output $y_{c,t}$ according to a production technology:

$$y_{c,t} = z_c l_{c,t}, \tag{3.6}$$

where $z_c \equiv 1$ denotes the fundamental productivity of country c and implies that all producers share the same level of productivity. These firms sell output to final good producers in all countries subject to trade costs:

$$y_{c,t} = \sum_{c'} d_{cc'} y_{cc',t}. \tag{3.7}$$

The profit maximization problem of the downstream good producers gives the constant markup pricing rule:

$$p_{cc',t} = \frac{\sigma}{\sigma - 1} \frac{w_{c,t}}{z_c}. \tag{3.8}$$

The optimal profit of each producer is

$$\pi_{c,t} = \sum_{c'} \pi_{cc',t}, \ \pi_{cc',t} = \frac{1}{\sigma} s_{cc',t} P^d_{c',t} Y^d_{c',t} \tag{3.9}$$

where the market share of each producer from country c in country c' is given by

$$s_{cc',t} = (\frac{d_{cc'} p_{cc',t}}{P^d_{c',t}})^{1-\sigma} = \frac{1}{T_{c,t} + T_{c',t} (\frac{d_{c'c'} w_{c',t} z_c}{d_{cc'} w_{c,t} z_{c'}})^{1-\sigma}}, \tag{3.10}$$

and the final good price can be rewritten as

$$P^d_{c,t} = T_{c,t}^{\frac{1}{1-\sigma}} (d_{cc} \frac{\sigma}{\sigma - 1} \frac{w_{c,t}}{z_c}) (1 + \frac{T_{c',t}}{T_{c,t}} (\frac{d_{c'c} w_{c',t} z_c}{d_{cc} w_{c,t} z_{c'}})^{1-\sigma})^{\frac{1}{1-\sigma}}. \tag{3.11}$$

Therefore, the total profits of downstream firms are

$$\Pi_{c,t} = T_{c,t}\pi_{c,t}, \tag{3.12}$$

and the total exports of downstream firms in country c to country c' are

$$\mathrm{EX}_{cc',t} = T_{c,t}d_{cc'}p_{cc',t}y_{cc',t} = T_{c,t}s_{cc',t}P^{d}_{c',t}Y^{d}_{c',t}. \tag{3.13}$$

3.1.4 Downstream Goods Innovation

In each country, an innovator purchases $Y^{rd}_{c,t}$ amounts of semiconductor goods $Y^{SA}_{c,t}$ to develop new technologies in downstream. Each technology is used to produce a unique variety. The stock of technologies available for production evolves according to

$$\dot{T}_{c,t} = \iota_c\left(\bar{T}_t - T_{c,t}\right) \; + \; \lambda^{d}_{c}\left(Y^{rd}_{c,t}\right)^{\alpha}T^{1-\alpha}_{c,t} \tag{3.14}$$

where $\bar{T}_t = \sum_c T_{c,t}$ is the world technology stock, $\iota_c \in [0,1]$ is the speed of knowledge diffusion from the global frontier, λ^{d}_{c} is country-specific downstream innovation efficiency, and $\alpha \in (0,1)$ governs the returns to R&D effort. The first term captures international spillovers, which will force all countries to share a common growth rate along the balanced growth path. The second term is a constant-returns-to-scale (in Y^{rd} and T) innovation function. As detailed later, we can guess and verify that the growth rate of technology stock g^d is equal to the semiconductor input growth g along the balanced growth path. The downstream R&D intensity

$$u_{c,t} \equiv \frac{Y^{rd}_{c,t}}{T_{c,t}} \tag{3.15}$$

is therefore constant on the balanced growth path.

The innovator owns all technologies in a country and the production profits of producers. The maximization problem of the innovator is as follows:

$$R_t V_{c,t} - \dot{V}_{c,t} = \max_{Y^{rd}_{c,t}} \left\{ \Pi_{c,t} - P^{SA}_{c,t}(1-\kappa_c)Y^{rd}_{c,t} + \frac{\partial V_{c,t}}{\partial T_{c,t}}\dot{T}_{c,t} \right\}. \tag{3.16}$$

where $\dot{V}_{c,t}$ denotes the derivative of $V_{c,t}$ with respect to time, $V_{c,t}$ denotes the value of the innovator, $P^{SA}_{c,t}$ denotes semiconductor price, and κ_c denotes innovation subsidy to downstream innovation. As shown later, the value of the innovator is linear in T: $V_{c,t} = v_{c,t}T_{c,t}$. Moreover, $V_{c,t}$ is constant along the balanced growth path. Hence $v_{c,t}$ declines at rate $-g^d$: $v_{c,t} = \tilde{v}_c e^{-g^d t}$ with $\tilde{v}_c$ constant. Using $V_{c,t} = v_{c,t}T_{c,t}$, $\partial V_{c,t}/\partial T_{c,t} = v_{c,t}$, and $\dot{T}_{c,t}$ from equation (3.14), the first-order condition with respect to $u_{c,t}$

$$u_{c,t} = \left(\frac{v_{c,t}\lambda_c^d \alpha}{P^{SA}_{c,t}(1-\kappa_c)} \right)^{\frac{1}{1-\alpha}}. \tag{3.17}$$

Therefore, the semiconductor price level $P^{SA}_{c,t}$ directly influences downstream R&D intensity while the semiconductor growth drives the long-run growth of downstream.[2]

3.1.5 Semiconductor Production

The semiconductor aggregate good $Y^{SA}_{c,t}$ is used as an innovation input and is non-tradable. $Y^{SA}_{c,t}$ is produced using a unit measure of heterogeneous semiconductor intermediates according to

$$Y^{SA}_{c,t} = \exp\left[\int_0^1 \ln(Y^s_{c,t})ds\right], \tag{3.18}$$

where $Y^s_{c,t}$ is a combination of both domestically produced and foreign-produced semiconductors according to

$$Y^s_{c,t} = \left(\sum_{c' \in \mathbb{C}} (y^s_{cc',t})^{\frac{\sigma^s - 1}{\sigma^s}} \right)^{\frac{\sigma^s}{\sigma^s - 1}}, \tag{3.19}$$

where $\sigma^s > 1$. Note that selling to foreign markets is subject to the export control policy, represented by an indicator $1_{\text{export ban}_{scc'}}$. If exporting is banned, the value of the indicator is 0, and if it is allowed, the value is 1. Additionally, exporters face iceberg trade costs $d^s_{cc'} \geq 1$. For each semiconductor

[2] As detailed later, $P^{SA}_{c,t}$ declines at rate $-g$ along the balanced growth path, and g is the semiconductor input growth rate.

intermediate, there is one semiconductor producer in each country with a production technology:

$$y^s_{c,t} = z^s_{c,t} l^p_{sc,t}, \tag{3.20}$$

where $y^s_{c,t}$, $z^s_{c,t}$, and $l^p_{sc,t}$ denotes output, productivity, and labor input of semiconductor intermediate s in country c at period t. Using foreign-produced semiconductors not only results in variety gains, but also in efficiency gains (higher supply and lower price) if foreign varieties are more productive.

Taking as given other producers' decisions, semiconductor intermediate producers choose goods price and labor input to maximize their profits in each destination market subject to trade policies, production technology, and demand from semiconductor aggregate good producers, leading to a markup price-setting rule in each destination market $c' \in \mathbb{C}$:

$$p^s_{cc',t} = \frac{\varepsilon^s_{cc',t}}{\varepsilon^s_{cc',t} - 1} \frac{w^{\text{semi}}_{c,t}}{z^s_{c,t}}, \tag{3.21}$$

where the demand elasticity is given by

$$\varepsilon^s_{cc',t} \equiv sh^s_{cc',t} + \sigma^s (1 - sh^s_{cc',t}), \tag{3.22}$$

$$sh^s_{cc',t} \equiv \frac{p^s_{cc',t} y^s_{cc',t}}{\sum_{c \in \mathbb{C}} d^s_{cc'} p^s_{cc',t} y^s_{cc',t}} = \left(\frac{p^s_{cc',t}}{P^s_{c',t}}\right)^{1-\sigma^s}, \tag{3.23}$$

$sh^s_{cc',t}$ denotes the market share of semiconductor intermediate s produced by country c in the destination market c', $d^s_{cc',t}$ denotes trade costs, $w^{\text{semi}}_{c,t}$ denotes the wage rate of semiconductor labor in country c. Consistent with previous literature (e.g., Atkeson and Burstein (2008)), semiconductor producers' pricing and production decisions depend only on the *relative productivity* among countries for each semiconductor intermediate s. A higher relative productivity leads to a lower price, higher market share, markup, output and production profits of semiconductors.

3.1.6 Semiconductor Innovation

Semiconductor producers make innovation investment to compete for higher profits by improving their productivity. Suppose that country c producing semiconductor intermediate s at time t has a technology level $z^s_{c,t} \equiv \lambda^{k^s_{c,t}}$, where $k^s_{c,t} \in \mathbb{N}$ represent the technology rungs of firms. The relative productivity between U and C is $\frac{z^s_{U,t}}{z^s_{C,t}} = \lambda^{k^s_{U,t} - k^s_{C,t}}$. Define $m_{s,t} \equiv k^s_{U,t} - k^s_{C,t}$ as the technology gap between U and C for producing semiconductor intermediate s. It can be shown that each s can be represented by m. For computational feasibility the technology gap is finite: $m \in \{-\bar{m}, ..., 0, ..., \bar{m}\}$.

Semiconductor producers' innovations follow a controlled Poisson process, with the arrival rate $e_{c,t}(m)$ determined by their innovation investment

$$R^{\text{semi}}_{c,t}(m) = \frac{\alpha^s_c(1-\kappa^s_c)}{\gamma} e_{c,t}(m)^\gamma l^i_{c,t}, \tag{3.24}$$

where $l^i_{c,t} \equiv 1$ units of final good are used for innovation investment, $\alpha^s_c > 0$ represents the scale of semiconductor innovation cost, $\gamma > 1$ implies innovation investment is convex in the arrival rate, and κ^s_c denotes the innovation subsidy by the government, a common policy in semiconductor industry across countries (cf. Goldberg, Juhász, Lane, Lo Forte, and Thurk (2024)). The specification implies that within a time interval Δt, the probability of an innovation occurring is $e_{c,t}(m)\Delta t + o(\Delta t)$, and the probability of more than one innovation arriving is $o(\Delta t)$.

Countries that are not in the global technology frontier also improve their productivity by getting knowledge spillovers from the global frontier. The knowledge spillovers across countries exist to ensure the existence of a non-degenerate equilibrium along the balanced growth path. Within a time interval Δt, a country receives knowledge spillovers freely with probability

$$\iota(m, 1_{c' \text{ exports to } c}, 1_{c \text{ not in the global frontier}}) = \begin{cases} \epsilon & \text{if} \quad 1_{c' \text{ exports to } c} = 0 \quad \text{or} \quad 1_{c \text{ not in the global frontier}} = 0, \\ \iota & \text{if} \quad 1_{c' \text{ exports to } c} = 1 \quad \text{and} \quad 1_{c \text{ not in the global frontier}} = 1, \end{cases}$$

where $\epsilon > 0$ is arbitrarily small and ensures the existence of a non-degenerate equilibrium.

We use a function $F_c(m, m')$ to summarize the productivity change due to innovation or getting knowledge spillovers for each country and consider a special case – productivity can only increase

by λ; we can generalize the innovation step size later on when it is necessary in quantitative analysis:

$$F_U(m, m') = \begin{cases} 1 & \text{if } m' = \min\{m+1, \bar{m}\}, \\ 0 & \text{otherwise,} \end{cases} \tag{3.25}$$

and symmetrically for other countries. Given others' decisions, the value function of country c is

$$R_t V^s_{c,t}(m) - \dot{V}^s_{c,t}(m) = \max_{e_{c,t}(m)\in[0,\bar{e}]} \{\Pi^s_{c,t}(m) P^{SA}_{c,t} Y^{SA}_{c,t} - P^d_{c,t} R^{\text{semi}}_{c,t}(m) \tag{3.26}$$

$$+(e_{c,t}(m) + \iota(m, 1_{c' \text{ exports to } c}, 1_{c \text{ not in the global frontier}})[F_c(m, m')V^s_{c,t}(m') - V^s_{c,t}(m)] \tag{3.27}$$

$$+ \sum_{c' \neq c} (e_{c',t}(m) + \iota(m, 1_{c' \text{ exports to } c}, 1_{c \text{ not in the global frontier}}))[F_{c'}(m, m')V^s_{c,t}(m') - V^s_{c,t}(m)], \tag{3.28}$$

where $\dot{V}^s_{c,t}(m)$ denotes the derivative of $V^s_{c,t}(m)$ with respect to time, $\Pi^s_{c,t}(m) P^{SA}_{c,t} Y^{SA}_{c,t}$ denotes the optimal production profit, $P^{SA}_{c,t} = \exp[\int_0^1 \ln(P^s_{c,t})ds]$ denotes the semiconductor price, and $P^s_{c,t} = (\sum_{c'} (d^s_{cc',t} p^s_{cc',t})^{1-\sigma^s})^{\frac{1}{1-\sigma^s}}$ denotes the price of semiconductor intermediate s. This results in the following optimal innovation decision:

$$e_{c,t}(m) = \left(\frac{[F_c(m, m')V^s_{c,t}(m') - V^s_{c,t}(m)] P^{SA}_{c,t} Y^{SA}_{c,t}}{\alpha^s_c (1 - \kappa^s_c) P^d_{c,t}} \right)^{\frac{1}{\gamma-1}}. \tag{3.29}$$

3.2 Equilibrium

In this section, we specify the equilibrium and key variables of interest.

3.2.1 Equilibrium Definition

A Balanced Growth Path (BGP) Equilibrium of the two-country economy consists of prices $\{R_t, w_{c,t}, w^{\text{semi}}_{c,t}, P^{SA}_c, P^d_c, p^s_{cc',t}, p_{cc',t}\}$, and allocations $\{Y^{SA}_c, Y^d_c, C_c, Y^{rd}_{c,t}, l^p_{sc,t}, e_{sc,t}, l_{c,t}, T_{c,t}, \mu_{s,t}\}$ such that for $c \in \mathbb{C}$, $s \in [0, 1]$ and all $t \in [0, \infty)$,

(i) households choose C_{ct} to maximize utility subject to budget constraints, pinning down R_{ct};

(ii) final good producers optimize profits to buy downstream intermediate goods $y_{cc',t}$;

(iii) downstream intermediate goods producers choose $l_{c,t}$, $p_{cc',t}$, $Y^{rd}_{c,t}$ to solve their pricing, employ-

ment, and semiconductor input usage decisions;

(iv) semiconductor aggregate good producers optimize profits to buy intermediates $y^s_{cc',t}$;

(v) semiconductor intermediate producers choose $p^s_{cc',t}$, $l^p_{sc,t}$, and $e_{sc,t}$ to solve their pricing, employment and innovation decision;

(vi) final good market clears in each country:

$$C_{c,t} = Y^d_{c,t} - \int_s R^{\text{semi}}_{sc,t} \mu_{s,t} ds; \tag{3.30}$$

(vii) downstream labor market clears in each country ($w_{US,t} \equiv 1$):

$$w_{c,t} L_c = w_{c,t} T_{c,t} l_{c,t}, \tag{3.31}$$

which can be rewritten as

$$w_{c,t} L_c = T_{c,t} \sum_{c'} \frac{\sigma - 1}{\sigma} s_{cc',t} P^d_{c',t} Y^d_{c',t}; \tag{3.32}$$

(viii) semiconductor labor market clears in each country:

$$w^{\text{semi}}_{c,t} L^{\text{semi}}_c = \sum_{c'} \int_s \frac{\varepsilon_{scc',t} - 1}{\varepsilon_{scc',t}} sh_{scc',t} \mu_{s,t} P^{SA}_{c',t} Y^{SA}_{c',t} ds; \tag{3.33}$$

(ix) the bond market clears:

$$\sum_c B_{c,t} = 0, \tag{3.34}$$

which determines R_{ct} via the household's Euler equation; $B_{c,t} = \bar{B}_c$, where $\bar{B}_c$ is a parameter to pin down steady state bond holdings;

(x) balance of payments hold:

$$EX_{cc',t} - EX_{c'c,t} + EX^{SA}_{cc',t} - EX^{SA}_{c'c,t} + R_{t-1} B_{c,t-1} - B_{c,t} = 0, \tag{3.35}$$

where $\text{EX}_{cc',t} = T_{c,t} s_{cc',t} P^d_{c',t} Y^d_{c',t}$, $\text{EX}^{SA}_{cc',t} = \int_s s_{scc',t} \mu_{s,t} ds P^{SA}_{c',t} Y^{SA}_{c',t}$;

and (xi) $T_{c,t}$ and relative productivity in semiconductor sector m evolve consistent with agents'

maximization problem and equation (3.14), ensuring a stationary distribution of firms over semiconductor technology gaps $\mu_t(m)$.

3.2.2 Semiconductor Technology Advantage

Define the U.S. semiconductor technology advantage

$$\text{S Tech Advantage}_{US,t} \equiv \sum_m m \cdot \mu_t(m), \tag{3.36}$$

where m represents the technology gap between U and C and $\mu_t(m)$ represents the distribution of semiconductor firms over the technology gap.

3.2.3 Downstream Technology Advantage

Define the U.S. downstream technology advantage

$$\text{S Tech Advantage}_{US,t} \equiv T_{US,t}/T_{CN,t}, \tag{3.37}$$

where $T_{c,t}$ represents the stock of downstream technologies in country $c \in \{U, C\}$.

3.2.4 Aggregate Growth

Define a semiconductor productivity index

$$Z_{c,t}^{SA} \equiv \int_0^1 \ln(z_{c,t}^s) ds, \tag{3.38}$$

where $z_{c,t}^s$ is the productivity of semiconductor firm for the intermediate s in country c at period t. Then we have

$$g \equiv g_{Z^{SA}} = [e_c(m)\mu(m) \cdot 1_{\text{c is global leader}} + \sum_c e_c(0)\mu(0)] \cdot \ln(\lambda), \tag{3.39}$$

$g_{Y_c^{SA}} = -g_{P_c^{SA}} = g_{Z_c^{SA}}$; $g_{w^{\text{semi}}} = g_{P_c^{SA} Y_c^{SA}} = 0$.

Note that

$$\ln(P_{c,t}^{SA}) = \int_0^1 \ln(P_{c,t}^s)ds = -Z_{c,t}^{SA} + CON_c, \tag{3.40}$$

where

$$CON_c = \frac{1}{1-\sigma^s}\int_0^1 \ln\left((\frac{\varepsilon_{cc,t}^s}{\varepsilon_{cc,t}^s-1}w_{c,t}^{\text{semi}})^{1-\sigma^s} + (d_{c'c}^s\frac{\varepsilon_{c'c,t}^s}{\varepsilon_{c'c,t}^s-1}w_{c',t}^{\text{semi}})^{1-\sigma^s}(\frac{z_{c',t}^s}{z_{c,t}^s})^{\sigma^s-1}\right)ds. \tag{3.41}$$

In the downstream sector, the productivity level ≡ stock of technology available for production $T_{c,t}$; the productivity growth g^d ≡ growth of $T_{c,t}$ (aggregate productivity growth); $g_{P_c^d Y_c^d} = g_{w_c^d} = 0$; $g_{s_{cc',t}} = -g^d$; $g_{P_c^d} = \frac{1}{1-\sigma}g^d = -g_{Y_c^d}$; $g_r = 0$. So $g_{\Pi_{c,t}} = g_{EX_{cc',t}} = 0$.

3.2.5 Export Controls

The export control indicator $1_{\text{export ban}_{scc'}} = 0$ can vary with semiconductor intermediate s, allowing for the analysis of export controls specifically on high-end semiconductors where the U.S. has a significant productivity advantage over China.

But in the baseline analysis, we consider an export control policy for all s.

3.2.6 Welfare

Welfare is measured by discounted sum of utility over time at time zero in each country. Specifically, the welfare of country c over horizon T at time t is

$$W_{c,t} = \int_t^{t+T} \exp(-\rho(s-t))\log(C_{c,s})ds. \tag{3.42}$$

We present the welfare effect of U.S. semiconductor export control (or more generally, the differences in welfare between a counterfactual and the baseline economy) in consumption equivalent terms as shown below:

$$\int_t^{t+T} \exp(-\rho(s-t))\log(C_{c,s}^{new})ds = \int_t^{t+T} \exp(-\rho(s-t))\log\left((1+\varsigma)C_{c,s}^{base}\right)ds. \tag{3.43}$$

This equation explains that if U.S. semiconductor export control at time t generates a new consumption path C_{cs}^{new} between t and $t+T$, it leads to a ς % variation in consumption-equivalent welfare over the horizon T. In other words, it results in a ς % increase in consumption at each point in time between t and $t+T$. In our quantitative analysis, we consider the welfare change in both the transition and the new BGP as $T \to \infty$.

3.3 Model Mechanism: Interplay between Semiconductor and Downstream

In this section, we discuss the model mechanism, focusing on how semiconductors and downstream goods interact in terms of production and innovation.

3.3.1 Semiconductor Innovation, Market Size Effect, and Input Cost Effect

The optimal innovation decision of semiconductor intermediate producers can be rewritten as

$$e_{c,t}(m) = \left(\frac{[F_c(m,m')v_{c,t}^s(m') - v_{c,t}^s(m)]P_{c,t}^{SA}Y_{c,t}^{SA}}{\alpha_c^s(1-\kappa_c^s)P_{c,t}^d} \right)^{\frac{1}{\gamma-1}}, \tag{3.44}$$

where $v_{c,t}^s(m) = \frac{V_{c,t}^s(m)}{P_{c,t}^{SA}Y_{c,t}^{SA}}$. It indicates that (i) higher $P_{c,t}^{SA}Y_{c,t}^{SA}$ leads to higher innovation incentive $e_{c,t}(m)$ (semiconductor market size effect), (ii) lower final good price $P_{c,t}^d$ leads to higher $e_{c,t}(m)$ (semiconductor innovation input cost effect), (iii) higher innovation subsidies lead to increased innovation incentives, which is straightforward, and (iv) innovation incentives vary with technology gaps across countries, as the additional profits from innovation vary with these gaps in the presence of market power. The technology-gap specific innovation incentive is consistent with previous step-by-step innovation literature (e.g., Aghion, Bloom, Blundell, Griffith, and Howitt (2005) and Sui (2023)). We now describe in detail the semiconductor market size effect and the semiconductor innovation input cost effect.

Semiconductor Market Size Effect. A higher semiconductor market size $P_{c,t}^{SA}Y_{c,t}^{SA}$ typically arises from stronger demand by downstream firms, as detailed below, and from a higher foreign market share when the domestic semiconductor technological advantage relative to the foreign country

increases.

Suppose there is a decline in foreign demand for semiconductors (for example, due to export controls). This lowers the demand for semiconductor production labor. In equilibrium, the semiconductor wage adjusts through the labor market clearing condition in the semiconductor sector. This typically leads to a lower semiconductor wage and hence a lower semiconductor price P^{SA}, according to Equation (3.21). The lower semiconductor price, in turn, raises the demand for semiconductors, partially offsetting the initial decline in demand caused by the export controls.

Semiconductor Input Cost Effect. Equation (3.11) implies that, all else equal, (i) a higher number of domestic technologies T_c or (ii) a higher number of foreign technologies relative to domestic technologies $\frac{T_{c'}}{T_c}$ contribute to a lower final goods price P_c^d.

3.3.2 Downstream Innovation, Input Cost Effect and Market Size Effect

Equation (3.17) characterizes the downstream firms' innovation incentives. A lower semiconductor price $P_{c,t}^{SA}$ leads to more innovation input and faster growth. This mechanism is supported by early empirical literature (e.g., Jorgenson (2001), Jorgenson, Ho, and Stiroh (2008)) which suggests that a decline in semiconductor prices leads to economy-wide growth. A higher downstream innovation efficiency λ_c^d also leads to higher innovation input and faster growth.

4 Quantitative Analysis

We will conduct a transition path analysis to account for both short-run and long-run effects, under the assumption that the world economy grows along balanced growth path prior to the introduction of unexpected, once-for-all export control policies. Short-run effects are defined as the impacts along the transition between the initial and the new balanced growth paths, while long-run effects are defined as the impacts after the economy has converged to the new balanced growth path. The numerical computation algorithm of the model fits standard macro model computation approaches and is detailed in Appendix A.

4.1 Parameterization

The parameterization serves to discipline two key mechanisms of the model: (i) links between semiconductor and downstream innovation across countries; (ii) links between semiconductor imports and downstream innovation across countries. The model parameters are jointly determined using the standard simulated method of moments technique, as detailed in Table 4.1. We source data from standard public datasets (e.g., World Bank), research papers (e.g., Goldberg, Juhász, Lane, Lo Forte, and Thurk (2024)), and our constructed dataset.

We primarily focus on U.S. data from the period 2015 to 2020 (unless specified) and assume that the differences across countries are based on innovation-related parameters. We estimate the model parameters in the initial balanced growth path. We estimate TFPR of semiconductor firms using standard Wooldridge (2009) method.

We run regressions in the model to match the estimates from the empirical counterpart. In the model, downstream firms' innovation efficiency, costs, and returns determine their incentives to purchase semiconductors, which in turn drive their own innovation and aggregate TFP growth. Greater semiconductor innovation lowers semiconductor prices and increases downstream purchases. Thus, aggregate TFP growth and the estimated regression coefficient β in (2.1) help discipline the effect of semiconductor innovation on downstream innovation. These effects can be country-specific, as innovation efficiency varies by country; therefore, estimating β in (2.1) separately for the U.S. (and its allies) and China disciplines the model. Additionally, since countries can import semiconductors instead of innovating domestically, the estimated β in (2.4) also helps discipline the semiconductor innovation's impact on downstream industries in the model.

4.2 Model Validation

Empirical estimates not used for calibration can be used for model validation.

Table 4.1: Parameterization

Parameters	Notation	Value	Targeted Moments	Data Source
Panel A. External Parameterization				
I. Households				
Discount factor	ρ	0.02	real interest rate	FRED
Bond adjustment cost	η	2	assigned	N.A.
Semiconductor labor	$L_c^{\text{semi}}, \forall c$	1	normalization	N.A.
II. Downstream Goods				
Elasticity of substitution	σ	5	common estimates	N.A.
Trade cost	$d_{cc'}, \forall c, c'$	1.1	average tariff rate	WITS
Innovation subsidy	κ	0	assigned	N.A.
III. Semiconductors				
Elasticity of substitution	σ^s	5	common estimates	N.A.
Trade cost	$d^s_{cc'}, \forall c, c'$	1.05	semiconductor tariff rate	WITS
Innovation input size	$l^i_c, \forall c$	1	normalization	N.A.
Innovation cost elasticity	γ	2	common estimates	N.A.
Innovation subsidy	κ^s	0	assigned	N.A.
Panel B. Internal Parameterization				
I. Households				
Bond holdings	$\bar{B}_U$		U.S. trade balance, % of GDP	World Bank
II. Downstream Goods				
Labor force	$L_c, \forall c$		Semiconductor output share in U.S.	
Innovation cost curvature	α		R&D-GDP ratio in U.S.	World Bank
Innovation efficiency	λ^d_U		Semi effect on downstream in U.S.	β in (2.1) for the U.S.
Innovation efficiency	λ^d_C		Semi effect on downstream in CN	β in (2.1) for China
Learning probability	$\iota_c, \forall c$		Semi imports effect on downstream	β in (2.4) for the U.S.
III. Semiconductors				
Productivity gap	λ		aggregate TFP growth	PWT
Innovation cost scale	α^s_U		share of industries with tech advantage	ORBIS
Innovation cost scale	α^s_C		global sales share of U.S. semi firms	ORBIS
Int'l knowledge spillover	ι		U.S. semi trade balance	UN Comtrade

Notes: This table summarizes the parameters and the moments that identify their values.

Table 4.2: Targeted Moments for Internal Parameterization

Targeted Moment	**Data**	**Model**
U.S. trade balance (1981–2020), % of GDP	-2.71	
2022 U.S. Semiconductor output, % of GDP	0.52	
U.S. R&D (1981–2020), % of GDP	2.61	
Effect of semi innovation on downstream innovation in U.S.	β in (2.1)	
Effect of semi innovation on downstream innovation in China	β in (2.1)	
Effect of semi imports on downstream innovation in U.S.	β in (2.4)	
Aggregate U.S. TFP growth % (1955–2020)	0.697	
Fraction of industries with semi tech advantage		
Global sales share of U.S. semiconductor firms		
U.S. semiconductor trade balance, % of GDP	-0.195	

Notes: This table summarizes the targeted empirical moments and their corresponding values used for model parameterization.

4.3 Counterfactual Analyses

In this section, we examine the effects of unexpected, permanent U.S. policies on the transition from the initial BGP equilibrium to the new BGP equilibrium.

Consider a case in which the U.S. has higher semiconductor innovation efficiency, higher downstream innovation efficiency and a greater semiconductor and downstream technological advantage than China. Assume that the economy is initially in a BGP equilibrium. We then introduce a U.S. semiconductor export control policy that reduces U.S. exports and the associated semiconductor knowledge spillovers to China to an infinitesimal level. We find that the transition from initial BGP to new BGP takes about 250 years to complete.

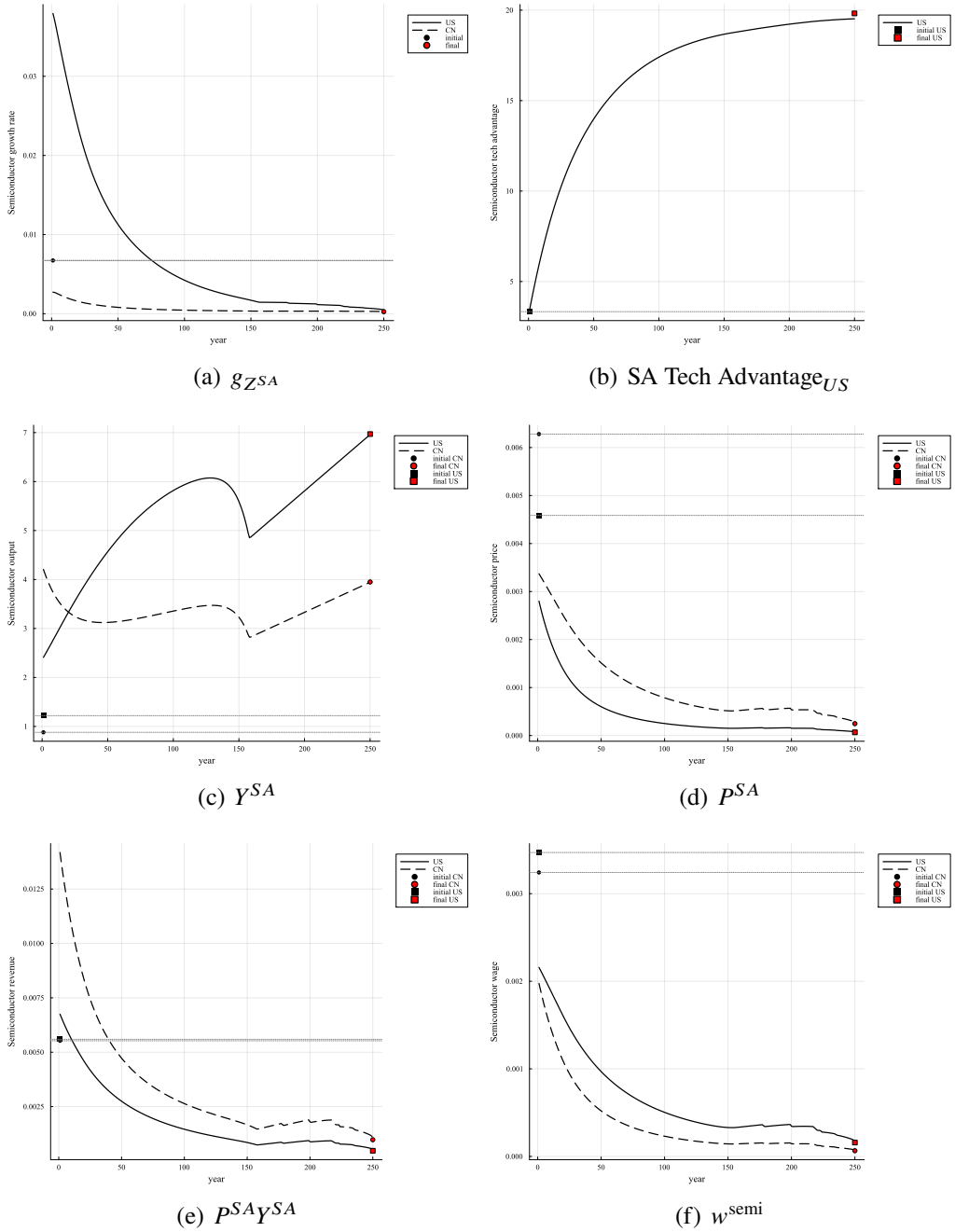
4.3.1 Effect of U.S. Semiconductor Export Control

Figures 4.1, 4.2 and 4.3 display the results.

In the U.S., on impact, U.S. semiconductor export controls lower the U.S. semiconductor wage rate because demand from China drops to zero. This, in turn, lowers U.S. semiconductor prices and raises U.S. downstream demand for semiconductors, increasing U.S. semiconductor production profits and supporting semiconductor innovation and growth. Reduced knowledge spillovers to China also strengthen U.S. semiconductor innovation and growth. In addition, the increased semiconductor supply to U.S. downstream firms boosts downstream innovation and growth.

In China, on impact, the semiconductor wage rate falls, which encourages higher domestic semiconductor production and supports downstream innovation. However, downstream growth remains lower than in the U.S. because China has lower downstream innovation efficiency. At the same time, China's semiconductor growth rate declines because reduced knowledge diffusion from the U.S. makes innovation more difficult for Chinese semiconductor producers. This innovation slowdown also dampens semiconductor output growth during the transition. In the long run, China falls behind in both the semiconductor and downstream sectors.

Figure 4.1: Effects of U.S. Semiconductor Export Control: Semiconductor



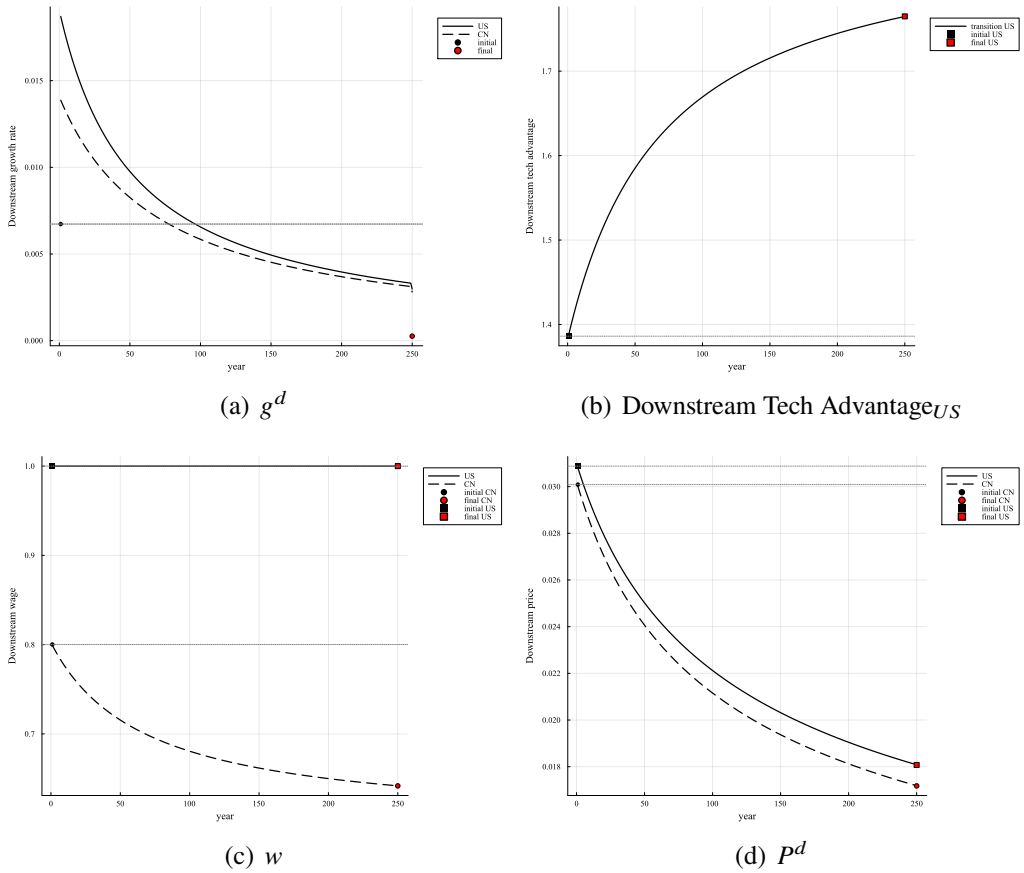
(a) $g_{Z^{SA}}$ (b) SA Tech Advantage$_{US}$

(c) Y^{SA} (d) P^{SA}

(e) $P^{SA}Y^{SA}$ (f) w^{semi}

Notes: The black and red circles represent the initial and new BGPs of the U.S., respectively. The black and red squares represent the initial and new BGPs of China, respectively. The black solid line shows the transition from the initial BGP to the new BGP for the U.S., while the black dashed line shows the corresponding transition for China.

Figure 4.2: Effects of U.S. Semiconductor Export Control: Downstream



(a) g^d (b) Downstream Tech Advantage$_{US}$

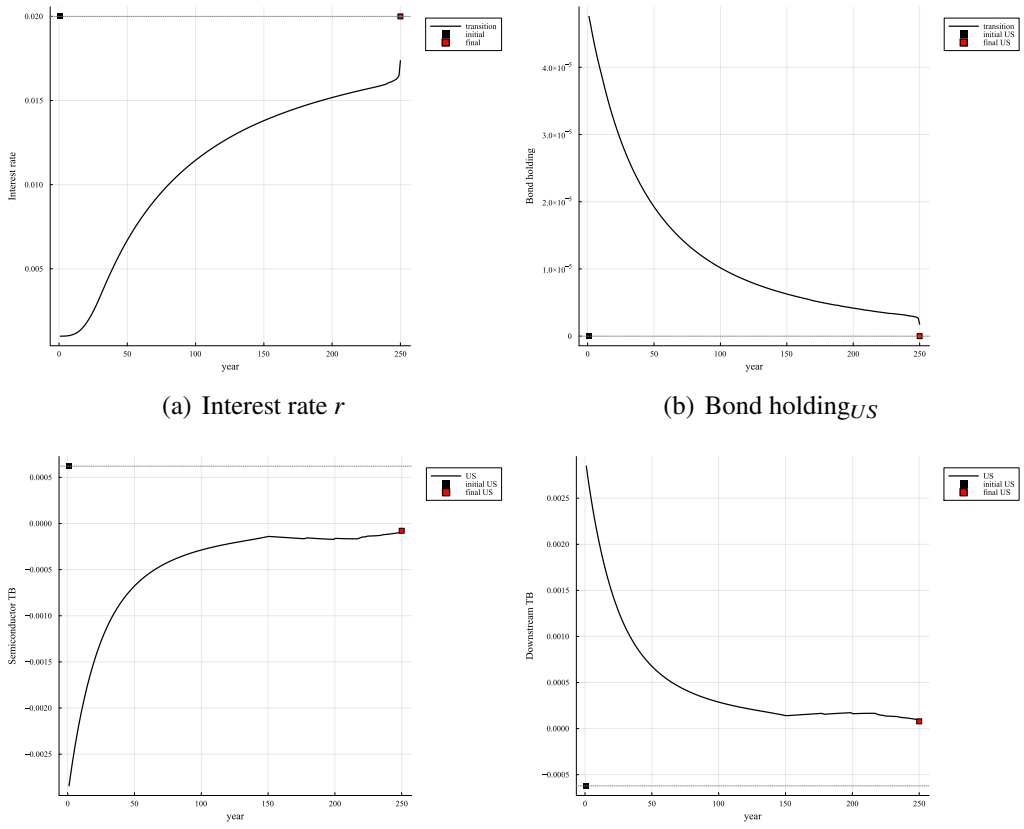
(c) w (d) P^d

Notes: The black and red circles represent the initial and new BGPs of the U.S., respectively. The black and red squares represent the initial and new BGPs of China, respectively. The black solid line shows the transition from the initial BGP to the new BGP for the U.S., while the black dashed line shows the corresponding transition for China.

4.3.2 Effect of U.S. Semiconductor Export Control when There is Positive Downstream Innovation Shock

Figures 4.4 and 4.5 show that in the presence of a positive downstream innovation shock to both countries, the semiconductor export control policy is more likely to increase downstream growth in the short run, thereby justifying the policy.

Figure 4.3: Effects of U.S. Semiconductor Export Control: Bond market and trade balance



(a) Interest rate r (b) Bond holding$_{US}$

(c) Semiconductor TB$_{US}$ (d) Downstream TB$_{US}$

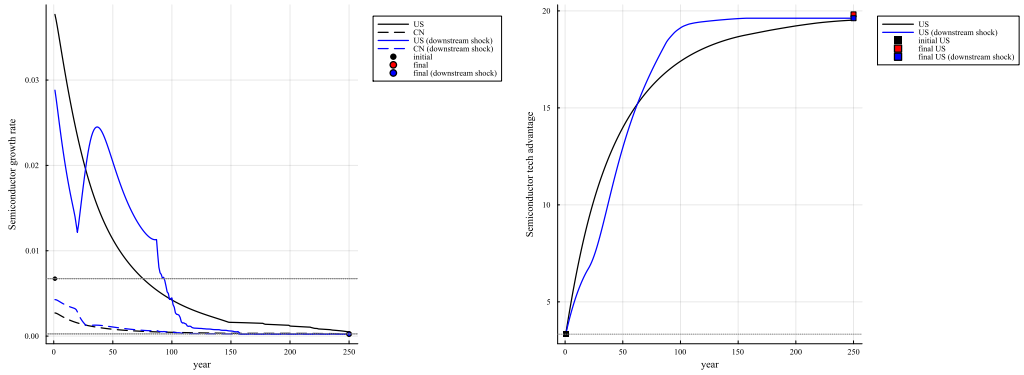
Notes: The black and red circles represent the initial and new BGPs of the U.S., respectively. The black and red squares represent the initial and new BGPs of China, respectively. The black solid line shows the transition from the initial BGP to the new BGP for the U.S., while the black dashed line shows the corresponding transition for China.

4.4 Additional Discussion

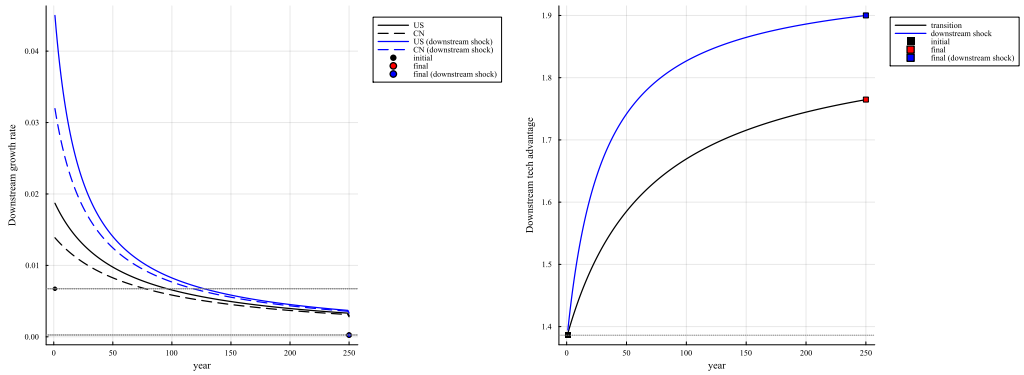
4.4.1 Decomposing the Effects of U.S. Semiconductor Export Controls

In the baseline analysis, the effects of U.S. semiconductor export controls are driven by both the reduction in semiconductor knowledge diffusion from the U.S. to China and the reduction in U.S. semiconductor exports to China. In this section, we instead model U.S. semiconductor export controls as only reducing U.S. semiconductor exports to China, to evaluate the short-run and long-run effects.

Figure 4.4: Effects of U.S. Semiconductor Export Control with Downstream Innovation Shock (1)



(a) $g_{Z^{SA}}$ (b) SA Tech Advantage$_{US}$



(c) g^d (d) Downstream Tech Advantage$_{US}$

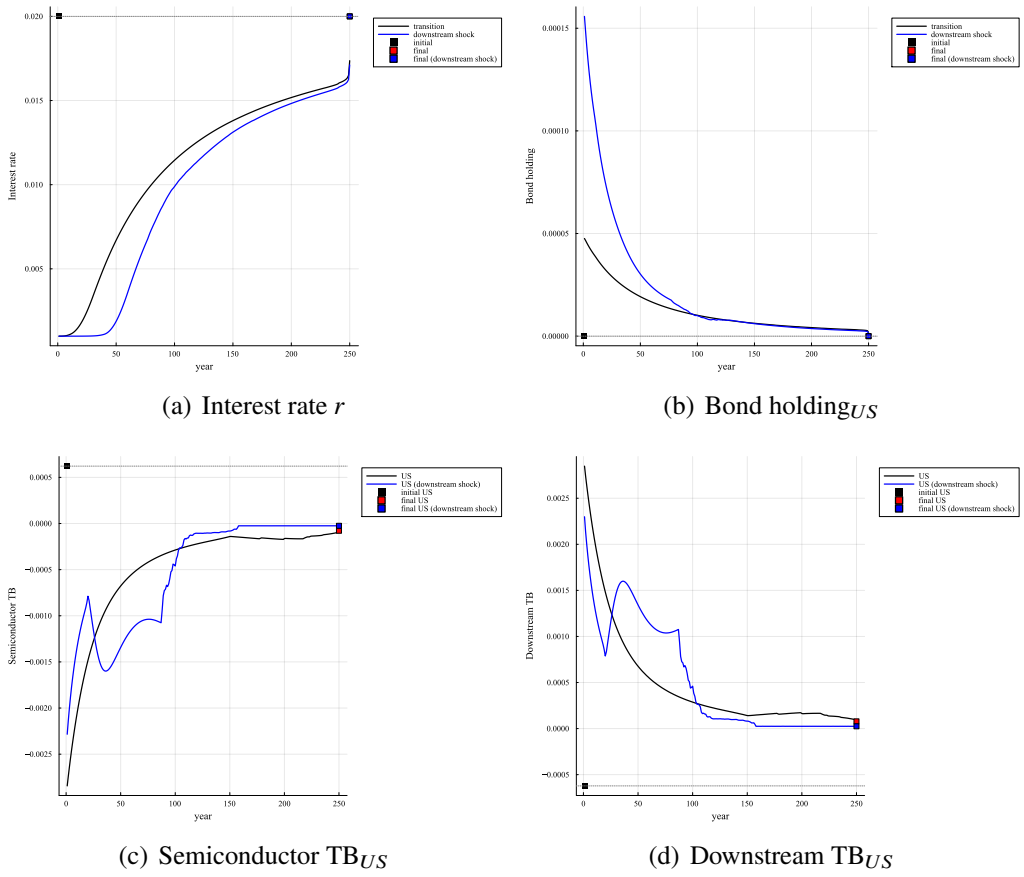
Notes: The black and red circles represent the initial and new BGPs of the U.S., respectively. The black and red squares represent the initial and new BGPs of China, respectively. The blue circles and squares represent the new BGPs resulting from both U.S. semiconductor export controls and a downstream innovation shock. The black solid line shows the transition from the initial BGP to the new BGP for the U.S., while the black dashed line shows the corresponding transition for China. The blue solid and dashed lines show the transitions from the initial BGP to the new BGPs under both U.S. semiconductor export controls and the downstream innovation shock.

4.4.2 Counterfactual Scenarios

If China significantly increases semiconductor innovation subsidies and downstream innovation subsidies. We find that the U.S. might not be able to increase its technological advantage over China in the long run; the short-run and long-run effects of U.S. semiconductor export controls are the same as in the baseline.

If the initial U.S. semiconductor technology advantage is high We find that the short-run positive growth effect on the semiconductor sector is significantly mitigated. This exercise highlights that when the initial U.S. semiconductor technology advantage is high, U.S. semiconductor export

Figure 4.5: Effects of U.S. Semiconductor Export Control with Downstream Innovation Shock (2)



(a) Interest rate r (b) Bond holding$_{US}$

(c) Semiconductor TB$_{US}$ (d) Downstream TB$_{US}$

Notes: The black and red circles represent the initial and new BGPs of the U.S., respectively. The black and red squares represent the initial and new BGPs of China, respectively. The blue circles and squares represent the new BGPs resulting from both U.S. semiconductor export controls and a downstream innovation shock. The black solid line shows the transition from the initial BGP to the new BGP for the U.S., while the black dashed line shows the corresponding transition for China. The blue solid and dashed lines show the transitions from the initial BGP to the new BGPs under both U.S. semiconductor export controls and the downstream innovation shock.

control policy is not favorable.

5 Conclusion

This paper studies the dynamic effects of U.S. semiconductor export controls in a two-country endogenous growth framework disciplined by new empirical evidence. Our quantitative analysis highlights a central intertemporal trade-off. U.S. export controls generate a *short-run boom* in U.S. semiconductor and downstream innovation: domestic semiconductor firms face stronger escape-competition incentives, and domestic downstream firms benefit from a temporary increase

in local semiconductor supply. At the same time, Chinese semiconductor innovation is immediately dampened by reduced access to frontier technologies and knowledge diffusion.

However, these gains do not persist. In the *long run*, the loss of access to the Chinese market reduces the scale of returns to U.S. semiconductor innovation, which then weakens innovation incentives in both the semiconductor sector and downstream industries. This long-run mechanism operates even in scenarios where the U.S. maintains or expands its technological lead over China. Hence, widening the technology gap is not sufficient to guarantee stronger long-run domestic innovation performance.

We further show that broader technological conditions matter for policy outcomes. A positive downstream innovation shock, such as rapid AI-related progress, amplifies short-run benefits and mitigates long-run losses from export controls, especially in downstream sectors. This result suggests that the macro-innovation environment can materially change the effectiveness of trade and technology restrictions.

Overall, our findings imply that semiconductor export controls should be evaluated as dynamic innovation policies rather than static trade measures. The short-run national innovation gains can coexist with long-run innovation costs, and complementary domestic policies (e.g., R&D support and downstream innovation capacity building) are critical for improving long-run outcomes. Future work can extend the framework to multi-country supply chains, endogenous policy responses by trading partners, and richer policy mixes that jointly target security and growth objectives.

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A Model Appendix

A.1 Model Derivations

A.1.1 Semiconductor Growth along BGP

Equation (3.39) defines the semiconductor productivity growth along BGP.

A.1.2 Semiconductor Growth in Transition Dynamics

Equation (3.38) defines the semiconductor productivity index $Z^{SA}_{c,t}$. The index is normalized to some level in the initial BGP. The evolution of the semiconductor productivity index along the transition is then determined by the semiconductor innovation decision rules and distribution of semiconductor firms.

The aggregate semiconductor price $P^{SA}_{c,t}$ can be derived as follows:

$$\ln(P^{SA}_{c,t}) = -Z^{SA}_{c,t} + \frac{1}{1-\sigma_s}\int_0^1 \ln\left((d^s_{cc}\frac{\varepsilon^s_{cc,t}}{\varepsilon^s_{cc,t}-1}w^{\text{semi}}_{c,t})^{1-\sigma_s} + (d^s_{c'c}\frac{\varepsilon^s_{c'c,t}}{\varepsilon^s_{c'c,t}-1}w^{\text{semi}}_{c',t}\frac{z^s_{c,t}}{z^s_{c',t}})^{1-\sigma_s}\right)ds. \tag{A.1}$$

A.1.3 Downstream Innovator's Problem: HJB and BGP Conditions

We derive the Hamilton-Jacobi-Bellman (HJB) equation for the downstream innovator, obtain the first-order condition (FOC), and simplify the system for a balanced growth path (BGP). The final equations are the ones used in the numerical solution.

Setup The stock of downstream technologies evolves as

$$\dot{T}_{c,t} = \iota_c\left(\bar{T}_t - T_{c,t}\right) \;+\; \lambda^d_c\left(Y^{rd}_{c,t}\right)^{\alpha}T^{1-\alpha}_{c,t}, \qquad \bar{T}_t = \sum_c T_{c,t}. \tag{A.2}$$

Define the R&D intensity $u_{c,t} \equiv Y^{rd}_{c,t}/T_{c,t}$. Then

$$\frac{\dot{T}_{c,t}}{T_{c,t}} = \iota_c\left(\frac{\bar{T}_t}{T_{c,t}} - 1\right) + \lambda^d_c u^\alpha_{c,t}. \tag{A}$$

The innovator receives total profit $\Pi_{c,t} = T_{c,t}\pi_{c,t}$, where $\pi_{c,t}$ is profit per variety from the final goods sector (taken as given). The innovator chooses $u_{c,t}$ to maximize firm value $V_{c,t}$.

HJB Equation In continuous time, the standard HJB equation is

$$R_t V_{c,t} = \max_{u_{c,t}} \left\{\Pi_{c,t} - P^{SA}_{c,t}(1-\kappa_c)Y^{rd}_{c,t} + \frac{\partial V_{c,t}}{\partial T_{c,t}}\dot{T}_{c,t} + \frac{\partial V_{c,t}}{\partial t}\right\}. \tag{A.3}$$

Assume linear homogeneity: $V_{c,t} = v_{c,t}T_{c,t}$. Then $\frac{\partial V_{c,t}}{\partial T_{c,t}} = v_{c,t}$ and $\frac{\partial V_{c,t}}{\partial t} = \dot{v}_{c,t}T_{c,t}$. Substituting these into the HJB equation yields:

$$R_t v_{c,t}T_{c,t} = \max_u \left\{T_{c,t}\pi_{c,t} - P^{SA}_{c,t}(1-\kappa_c)u_{c,t}T_{c,t} + v_{c,t}\dot{T}_{c,t} + \dot{v}_{c,t}T_{c,t}\right\}. \tag{A.4}$$

Subtracting $\dot{v}_{c,t}T_{c,t}$ from both sides and dividing by $T_{c,t}$, we obtain the intensive-form HJB equation:

$$R_t v_{c,t} - \dot{v}_{c,t} = \max_u \left\{\pi_{c,t} - P^{SA}_{c,t}(1-\kappa_c)u_{c,t} + v_{c,t}\frac{\dot{T}_{c,t}}{T_{c,t}}\right\}. \tag{HJB2}$$

The term $\frac{\dot{T}_{c,t}}{T_{c,t}}$ is given by (A) and depends on $u_{c,t}$.

First-Order Condition (FOC) Take the derivative of the right-hand side of (HJB2) with respect to $u_{c,t}$:

$$\frac{\partial}{\partial u}\left[-P^{SA}_{c,t}(1-\kappa_c)u_{c,t} + v_{c,t}\left(\iota_c(\bar{T}_t/T_{c,t} - 1) + \lambda^d_c u^\alpha_{c,t}\right)\right] = -P^{SA}_{c,t}(1-\kappa_c) + v_{c,t}\lambda^d_c \alpha u^{\alpha-1}_{c,t} = 0. \tag{A.5}$$

Thus, the optimal R&D intensity satisfies:

$$P^{SA}_{c,t}(1-\kappa_c) = v_{c,t}\lambda^d_c \alpha u^{\alpha-1}_{c,t}. \tag{FOC}$$

HJB on the Balanced Growth Path On a BGP, all real variables grow at constant rates. Let g be the common growth rate (equal to the semiconductor productivity growth rate). Since aggregate firm value V is stationary (constant) along the BGP but T grows at rate g, the value per variety $v_{c,t} = V/T$ must decline at rate g. Hence, $\dot{v}_{c,t} = -gv_{c,t}$.

Furthermore, $R_t = \rho$ (from the household's Euler equation with zero bond holdings), and $\dot{T}_{c,t}/T_{c,t} = g$. Substituting these into (HJB2), we get:

$$\rho v_{c,t} - (-gv_{c,t}) = \pi_{c,t} - P_{c,t}^{SA}(1-\kappa_c)u_{c,t} + v_{c,t}g \tag{A.6}$$

$$\rho v_{c,t} + gv_{c,t} = \pi_{c,t} - P_{c,t}^{SA}(1-\kappa_c)u_{c,t} + gv_{c,t} \tag{A.7}$$

The growth terms $gv_{c,t}$ perfectly cancel out on both sides, leaving the stationary HJB for the BGP:

$$\rho v_c = \pi_c - P_c^{SA}(1-\kappa_c)u_c. \tag{HJB-BGP}$$

Combining FOC and HJB-BGP From (FOC) we can solve for v_c:

$$v_c = \frac{P_c^{SA}(1-\kappa_c)}{\lambda_c^d \alpha u_c^{\alpha-1}}. \tag{3}$$

Insert this into (HJB-BGP) to obtain a relation between u_c, π_c, and the other parameters:

$$\rho \frac{P_c^{SA}(1-\kappa_c)}{\lambda_c^d \alpha u_c^{\alpha-1}} = \pi_c - P_c^{SA}(1-\kappa_c)u_c. \tag{A.8}$$

The system is closed by the growth equation (A) and the profit π_c from the final goods sector.

Summary of BGP Equations For each country c, the BGP equilibrium must satisfy the following simultaneous equations:

$$g = \iota_c\Big(\frac{\bar{T}}{T_c} - 1\Big) + \lambda_c^d u_c^\alpha, \tag{GE}$$

$$P_c^{SA}(1-\kappa_c) = v_c \lambda_c^d \alpha u_c^{\alpha-1}, \tag{FOC}$$

$$\rho v_c = \pi_c - P_c^{SA}(1-\kappa_c)u_c, \tag{HJB-BGP}$$

$$\pi_c = \frac{1}{\sigma}\sum_{c'} s_{cc'}\tilde{P}_{c'}^d \tilde{Q}_{c'}^d, \tag{Profit}$$

$$w_c L_d^c = \frac{\sigma-1}{\sigma} T_c \sum_{c'} s_{cc'}\tilde{P}_{c'}^d \tilde{Q}_{c'}^d, \tag{LM}$$

$$\tilde{P}_c^d = \left[T_c\Big(\frac{\sigma}{\sigma-1}\frac{w_c}{z_c}\Big)^{1-\sigma} + T_{c'}\Big(d_{c'c}\frac{\sigma}{\sigma-1}\frac{w_{c'}}{z_{c'}}\Big)^{1-\sigma}\right]^{\frac{1}{1-\sigma}}, \tag{Price Index}$$

$$\tilde{Q}_c^d = \left[T_c\big(\tilde{P}_c^d/p_{cc}\big)^{-\sigma} + T_{c'}\big(\tilde{P}_c^d/(d_{c'c}p_{c'c})\big)^{-\sigma}\right]^{\frac{\sigma}{\sigma-1}}, \tag{Final Output}$$

where $p_{cc'} = \frac{\sigma}{\sigma-1}\frac{w_c}{z_c}$ and $p_{c'c} = \frac{\sigma}{\sigma-1}\frac{w_{c'}}{z_{c'}}$. The semiconductor sector provides g, P_c^{SA}, and the market shares $s_{cc'}$ (through the price indices) as exogenous inputs.

A.1.4 Downstream Growth along BGP

Detrending and stationary system Define detrended variables that are constant on the BGP:

$$\tilde{T}_c = T_{c,t}e^{-gt}, \qquad \tilde{Y}_c^{rd} = Y_{c,t}^{rd}e^{-gt}, \qquad \tilde{P}_c^{SA} = P_{c,t}^{SA}e^{gt}, \qquad \tilde{P}_c^d = P_{c,t}^d e^{gt}, \qquad \tilde{Y}_c^d = Y_{c,t}^d e^{-gt},$$

and the stationary value per unit of detrended technology $\tilde{v}_c = v_{c,t}e^{gt} = V_c/\tilde{T}_c$ (since V_c is constant). The R&D intensity $u_c = \tilde{Y}_c^{rd}/\tilde{T}_c$ is also constant.

In terms of these, on the BGP ($\dot{\tilde{T}}_c = 0$)

$$\iota_c\Big(\frac{\bar{\tilde{T}}}{\tilde{T}_c} - 1\Big) + (\lambda_c^d)^{\omega_1} u_c^\alpha = g. \tag{1}$$

Common BGP across countries Equation (1) holds for each country. For a common g to be feasible, the right-hand sides must be equal for $c = U, C$. The diffusion terms $\iota_c(\bar{\tilde{T}}/\tilde{T}_c - 1)$ adjust so that this equality holds, given the country-specific λ_c^d and the endogenous u_c determined by (2)–(3)

and the rest of the equilibrium. Hence all countries share the same long-run growth rate g.

A.1.5 Downstream Growth in Transition Dynamics

TBD.