When Protectionism Kills Talent*

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Abstract

Could protectionist policies intended to revitalize domestic manufacturing instead weaken its core strengths: skilled workforce, innovation capacity, and talent pipeline? In the US chip manufacturing industry, we show that science and engineering employment has declined in response to protectionist measures—particularly in entry-level roles and at firms exposed to tariffs and reliant on foreign talent. Patent output fell and recruitment shifted overseas, while fewer domestic students pursued chip-related degrees, reducing the US share of global chip manufacturing expertise. Our conceptual framework shows that high proportions of foreign workers and inelastic labor supply contribute to the adverse effects of protectionist policies.

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1 Introduction

The US manufacturing landscape has recently seen significant changes, notably marked by the government's turn toward protectionism in 2018 (Fajgelbaum et al., 2020). Trade tariffs were introduced to revitalize domestic manufacturing and stimulate job creation and industry growth. As US firms adjusted to tariff-induced economic pressures, their hiring and workforce management strategies were further complicated by a tightening supply of skilled labor. The 'Buy American and Hire American' Executive Order, in particular, reduced the appeal of the US to international students and professionals, especially engineers and scientists, aspiring to contribute to the US workforce (Song and Li, 2022).[1]

In this paper, we examine the impact of these protectionist policies on the domestic labor markets within the US manufacturing sector, with a particular focus on the semiconductor (chip) industry. The chip industry is our focal point due to its strategic importance and significant vulnerability to tariffs, as a result of its intricate global supply chains and trade dependencies.[2] In addition, the sector's reliance on skilled and specialized international talent makes it particularly sensitive to changes in immigration policies and domestic labor market challenges. These factors make the chip manufacturing industry an ideal setting for exploring the impact of economic protectionism on workforce composition and adaptation.

The effects of protectionist policies on manufacturing firms are not clear ex ante. On

[1] See http://on.wsj.com/4fCTcUC, http://politi.co/4lo5nps., http://bit.ly/4maUYhY, and http://bit.ly/3Hs5WR8.

[2] Some of the semiconductor-related products affected by the tariffs include HS Codes 8486.20 (machines and apparatus for the manufacture of semiconductor devices or of electronic integrates circuits), 8486.90 (machines and apparatus of a kind used for the manufacture of semiconductor boules or wafers, etc.), 8541.90 (parts, diodes, transistors parts of diodes, transistors and similar semiconductor devices), and 8542.31 (processors and controllers, electronic integrated circuits). Countries subject to such tariffs include China, Taiwan, South Korea, Japan, the Netherlands, Germany, and India, in addition to 50 other countries. Source: http://www.econ.ucla.edu/pfajgelbaum/rtp_update.pdf. See also https://bit.ly/4a5aoyc.

the one hand, these policies could increase the demand for local workers by encouraging companies to invest more in domestic talent and training programs. This shift toward prioritizing local workforce utilization might enhance the productivity and self-sufficiency of the domestic labor market within the semiconductor industry. On the other hand, increased tariffs and potential retaliatory measures from other countries could make companies more cautious in hiring, possibly reducing recruitment and making hiring more selective. Stricter immigration policies could further constrain the supply of specialized and skilled workers, resulting in a labor shortage and hindering firms from fully benefiting from the intended stimulus of protectionist policies. These may ultimately lead to a decrease in employment. We develop a conceptual framework to formalize plausible effects. In our model, protectionist policies designed to revitalize domestic manufacturing and employment can produce opposite outcomes, with particularly severe effects in markets characterized by high reliance on foreign workers and inelastic labor supply, key features of the chip manufacturing industry.

We empirically test our model's predictions by leveraging a comprehensive dataset containing detailed employee-job-employer relationships for millions of individuals employed in this sector globally. Our data allows us to examine the impact of US protectionist policies on the employment landscape for scientists and engineers within US chip manufacturing firms, contrasting it with other job categories within the same firm-year. Our analysis reveals a notable downturn in employment indicators within these firms following the implementation of protectionist measures in 2018. Specifically, we observe a 9% reduction in the recruitment of scientists and engineers, accompanied by reduced attrition, which together contribute to a 3% reduction in the total workforce size. To provide context, the chip manufacturing sector in the US faces an annual loss of 2,285 science and engineering positions. Between 2019

and 2022, this results in a cumulative reduction of 9,140 jobs within the industry, which employed 76,150 scientists and engineers during this period.

The reduction in hiring occurs despite an increase in job postings for scientists and engineers and is primarily driven by sharp declines in R&D scientist roles and specialized manufacturing positions, such as piping and strain engineering, which are essential to improve chip performance. It is also especially acute in entry-level and junior positions, indicating that protectionist policies disproportionately affect those new to the workforce, potentially impacting the industry's future talent pipeline. Importantly, additional tests provide evidence that our results are not driven by recent trends in career transitions of data scientists and software engineers within the US chip manufacturing industry, who are the most likely to move into similar roles in other industries. This finding rules out the possibility that our observed effects merely reflect a broader shift in tech talent towards other sectors. Instead, it reinforces that protectionist policies are having a unique and significant impact on the chip manufacturing industry's labor market dynamics.

Beyond workforce disruptions, we document substantial innovation losses that threaten US technological competitiveness. Patent filings at US chip manufacturers decline by 15% following protectionist policies, with patent grants falling by 14%. Firms historically dependent on H-1B workers experience an additional 23% contraction in patent grants. These findings reveal that workforce constraints translated directly into reduced R&D output, suggesting that protectionist measures may have inadvertently undermined the technological foundations essential for maintaining competitive advantage in global chip markets. Complementing these innovation losses, we observe a fundamental shift in the global distribution of critical chip manufacturing skills, with the US losing over 5% of its skill concentration.

We also study how the workforce composition of US chip manufacturers changes across their segments around the world (i.e., at the firm-country-job category-year level) and based on their tariff exposure and reliance on foreign talent, particularly through the H-1B program. Our findings indicate that US chip manufacturers reduce their domestic science and engineering workforce in the US and increase their hiring of more experienced workers outside the US, particularly for both junior and mid-senior roles, reflecting an unintended consequence of US protectionist measures on domestic segments.

The employment effects in the US remain robust after controlling for high-dimensional fixed effects that capture a range of unobserved factors. These include yearly shocks at the firm–job category level (e.g., changes in a firm's demand for specific roles, shifts in the labor supply the firm faces for each job category, or the firm's annual exposure to automation or technologies such as AI that may increase or reduce the need for certain roles), as well as persistent characteristics at the firm–job category–country level. We also control for broader country–year shocks (e.g., changes in macroeconomic conditions, national industrial policies, and COVID-related disruptions) and local labor-market dynamics (e.g., firm-level exposure to yearly shocks in headquarters regions, persistent differences in the types of roles firms headquartered in specific locations tend to hire for, and year-to-year changes in demand or supply for particular job categories within each headquarters metro area).

The reduction in US science and engineering hiring is most pronounced in firms that sponsored H-1B petitions before the ban. This finding reflects US firms' reliance on international labor markets and the critical science and engineering expertise provided through H-1B visas. Among the countries where US chip firms have expanded their presence are Canada, which introduced favorable visa policies (Esterline, 2023), and European countries such as

the Netherlands, which has an established chip manufacturing industry. Furthermore, firms with greater exposure to tariffs experience stronger distortions in science and engineering roles, which are closely tied to R&D and manufacturing processes reliant on global supply chains and specialized raw materials. This is consistent with higher input costs from tariffs raising production expenses, prompting firms to reduce investments in R&D-intensive positions, where costs are typically concentrated (Martin and Otto, 2024).

Finally, we analyze the educational and career outcomes of cohorts with chip manufacturing skills. Using a difference-in-differences approach, controlling for shocks at the country-degree-job category, country-year and degree-year levels, we find a 15% decline in the number of classmates entering engineering or scientist roles alongside individuals with chip-related expertise after the implementation of US protectionist policies in 2018. Using Department of Education data, we extend our analysis to distinguish between US residents and non-residents and find that completion of bachelor's and pre-bachelor's degrees in chip manufacturing has declined significantly for both groups post 2018. This finding indicates a broader waning interest in chip-related fields within the US education system. Overall, these trends suggest a concerning shrinkage in the talent pipeline for the chip manufacturing industry, with fewer students choosing or persisting in careers within this critical sector.

Our analysis reveals particularly stark effects on international students, who experience 17-29% reductions in chip manufacturing-related degree completions, indicating that immigration policy uncertainty creates immediate deterrent effects on global talent attraction. Among domestic graduates who do complete technical programs, we observe increasing migration toward alternative careers in finance and consulting, creating a dual challenge for the US chip manufacturing industry: fewer students entering relevant fields combined with fiercer

competition among firms to persuade the remaining students to stay in the industry. These educational and career trajectory shifts, validated through both self-reported LinkedIn data and official Department of Education records, suggest that the talent pipeline constraints documented in our workforce analysis may intensify over time as reduced domestic interest compounds with diminished international participation.

We build on the literature studying high-skilled immigration and innovation, while also connecting to broader work on trade frictions and economic nationalism. The literature on high-skilled immigration and innovation has primarily examined the effects of immigration restrictions on the directly affected firms or individuals. Kerr and Lincoln (2010) use visa lottery variation to show that restrictions reduce patenting by ethnic inventors, while Chen et al. (2021), Doran et al. (2022) and Dimmock et al. (2022) employ similar lottery-based identification to study firm-level effects. More recently, Glennon (2024) demonstrates that H-1B restrictions increase foreign affiliate employment, and Bernstein et al. (2024) show that immigrants produce quarter of the innovation output in the US. Our paper contributes to this literature in several important ways. First, while lottery-based identification strategies focus on the effects of immigration policy on marginal H-1B applicants, our analysis captures broader industry-level equilibrium effects—including indirect impacts on firms that are not heavily reliant on H-1B workers. Second, beyond measuring contemporaneous impacts on individuals and firms, we trace the full trajectory from educational decisions to career outcomes and innovation, highlighting how policy can shape long-term talent development. We provide new evidence on how protectionist policies influence domestic students' career interests and attract or deter international student enrollment—factors that can reinforce or redirect the flow of high-skilled talent. These forward-looking effects underscore

the potential for policy to reshape the innovation pipeline and talent landscape over time. Taken together, our analysis offers the first comprehensive view of how broad protectionist measures—encompassing both immigration restrictions and trade barriers—jointly influence workforce composition, skill distribution, innovation capacity, educational pathways, and global talent allocation in a key manufacturing industry.

The extensive literature on the *China shock* provides further context for understanding large-scale import competition effects. Autor et al. (2014) document adverse effects of increased Chinese imports between 1992 and 2007 on employment, labor force participation, and wages in competing manufacturing industries, with higher-wage workers experiencing relatively better outcomes. Pierce and Schott (2016), Autor et al. (2013), Acemoglu et al. (2016), Caliendo et al. (2019), and Autor et al. (2021) extend this analysis across broader outcomes and time periods. At the firm level, Cen et al. (2023) show how US companies used internal capital markets to stay resilient to China's five-year plans, often by shifting production or offshoring to supported Chinese industries. Hombert and Matray (2018) find that while Chinese imports generally slow growth and reduce profitability, firms with more R&D experience smaller disruptions due to increased product differentiation.[3] While this extensive literature provides crucial insights into how external economic pressures affect domestic industries, less attention has been paid to the intersection of trade policy with immigration restrictions—particularly how these dual pressures affect high-skilled industries dependent on global talent networks, which we focus on in this paper.

Our findings also contribute to the growing literature on economic nationalism and its

[3]Also see Bernard et al. (2012, 2006); Frésard and Valta (2016); Xu (2012); Valta (2012) on the effects of imports on leverage, cost of debt, capital investments, and outsourcing. Juhász et al. (2023) and Juhász and Lane (2024) provide detailed reviews on industrial policy effectiveness. See Hoberg and Phillips (2016) on product differentiation.

unintended consequences. Dinc and Erel (2013) document prevalent economic nationalism in European merger responses, where authorities prefer domestic over foreign ownership. In financial markets, Morse and Shive (2011) examines patriotism's impact on equity investments, while Gupta and Yu (2007) studies bilateral capital flows. Most relevant to our work, D'Acunto et al. (2023) show that the 2007 Employ American Workers Act led to reduced patent filings in FinTech, cybersecurity, and payment systems, alongside increased wage premiums for retained foreign workers. Additionally, Hankins et al. (2025) show that auto manufacturers passed a significant share of the 2018 metal-tariff costs on to consumers through higher captive-finance interest rates, particularly affecting consumers with less elastic credit demand and in areas with lower credit market competition. Building on this foundation, our study shows that protectionist policies in globally integrated, knowledge-intensive industries can produce self-defeating outcomes, reducing high-skill employment, pushing talent and innovation abroad, and weakening the US position in global talent markets. Industries embedded in international talent networks and supply chains are particularly vulnerable to such backfire effects, which reverberate through educational institutions, labor markets, and innovation ecosystems. By tracing effects across the entire talent development lifecycle—from education and career entry to advanced innovation—we capture dynamics that can create lasting structural damage even after policies are reversed. This comprehensive view of protectionist policy effects across multiple dimensions provides novel insights that previous literature examining individual channels in isolation could not capture.

1.1 Why Chip Manufacturing Industry?

The broad impact of protectionist policies likely extended to many US manufacturing sectors. We focus on the chip manufacturing sector for three reasons.[4] First, the chip manufacturing industry relies heavily on international talent (Ozimek and O'Brien, 2023) and collaboration for innovation and competitiveness (Jones and Lotze, 2023; Bown and Wang, 2024). Protectionist measures, such as immigration restrictions, disrupt talent flows and hinder international collaboration, limiting the industry's ability to innovate. Second, the chip manufacturing industry operates in a highly interconnected global supply chain (Thadani and Allen, 2023). Tariffs on imported materials raise production costs for chip manufacturers, reducing their global competitiveness. Retaliatory tariffs from trading partners simultaneously decrease foreign demand for US chip products, compounding negative effects on the industry's profitability and growth prospects. These trade barriers primarily disrupt manufacturing, with weaker direct effects on design. Third, our aim is to trace the career trajectories of individuals and identify their skill sets. Analyzing how individuals adapt their careers to protectionist shocks requires examining millions of resumes. Our data is especially appropriate for studying the chip industry, as many workers in this industry voluntarily disclose their information, which is not commonly observed in other manufacturing sectors.[5]

Taken together, the chip manufacturing sector provides a useful laboratory for examining the influence of protectionist policies on globally integrated, high-tech manufacturing

[4]There are not many papers studying the dynamics of workforce in specific industries. The closest study to ours is Angel (1989) which investigates the labor market and the geographic concentration of engineers in the US semiconductor sector.

[5]The top three industries that constitute the greatest number of resumes on this platform are financial services, information technology and services, hospital & health care.

sectors. Its economic importance, sensitivity to visa and tariff shocks, and rich data availability allow precise measurement and credible empirical analysis. These features provide the granular, industry-specific variation emphasized by the New Empirical Industrial Organization tradition, which favors avoiding cross-industry analyses that often complicate inference (Bresnahan (1989); Einav and Levin (2010)). This approach has been influential across fields, including recently in financial economics (e.g., Cookson (2017, 2018); Hankins et al. (2025)).

2 Conceptual Framework

To motivate and provide a framework for interpreting our empirical findings, we introduce a model in which consumers demand chips and other goods, and chip firms decide on hiring and production amid protectionist policies. We demonstrate that protectionist policies can lead to reduced hiring and production by US chip firms. In particular, the decline is most pronounced when the sector relies heavily on foreign workers and inelastic labor supplies.

Demand for Chip Products

There is a representative consumer who demands both chips and other products, which we denote by Y_C and Y_O, respectively. We assume that the consumer has a standard CES (constant elasticity of substitution) utility, like in Fajgelbaum et al. (2020). The consumer chooses the consumption bundle to maximize its utility:

$$u = \max_{Y_C, Y_O} \left(\alpha_C^{\frac{1}{\eta}} Y_C^{\frac{\eta-1}{\eta}} + \alpha_O^{\frac{1}{\eta}} Y_O^{\frac{\eta-1}{\eta}} \right)^{\frac{\eta}{\eta-1}}, \tag{1}$$

subject to the budget constraint:

$$Y_C \times P_C + Y_O \times P_O = I, \tag{2}$$

where α_C and α_O are the share parameters corresponding to chips and the bundle of other products in the consumer's utility function. I is the consumer's budget constraint.

We model the supply of other products as perfectly elastic at a price of P_O, treated as exogenous, primarily to simplify our equilibrium calculations. The main intuitions remain the same if the supply is elastic. Chip products are supplied by J symmetric US firms, whose production decisions are detailed below.

Production Environment

A chip manufacturer uses domestic and foreign labor as inputs to produce chip products under a production function: $y = zL^{\theta}$, where z represents the firm's total factor productivity (TFP), and L represents workers hired by the firm. We do not explicitly include capital in the production function, assuming instead that firms rent productive capital from a competitive market, with these decisions optimized out.

The firm chooses its employment to maximize profit, net of wage costs.

$$\pi_j = \max_L P_C(1-v)zL^{\theta} - WL, \tag{3}$$

where P_C represents the market price for chip products, and v denotes the percentage of variable cost, covering costs such as raw materials, shipping, delivery, and utilities, and

finally, W represents the wage rate.

Taking the first-order condition of the firm's profit with respect to domestic and foreign employment yields the firm's optimal labor demand:

$$(1-v)zP_C\theta L^{\theta-1} = W, \tag{4}$$

which suggests that, in equilibrium, the wage rate paid by the firm should equal its marginal revenue product of labor.

The Repercussions of Protectionist Policies

We model the effects of protectionist policies through three primary channels. First, they provide investment subsidies, targeting R&D and talent development programs, which enhance a firm's TFP and increase the marginal productivity of labor. Second, these policies impose tariffs on raw materials and intermediate inputs imported from abroad, raising domestic firms' variable costs (v) and thereby reducing their profit margins. Lastly, protectionist policies limit firms' access to labor, particularly foreign workers. The labor supply curve faced by US firms is $S(\cdot)$, and protectionist policies shift it inward to $\lambda S(\cdot)$, with $\lambda < 1$.

The Equilibrium

Proposition 1. *There is a unique combination of equilibrium wage rate, W, and price for chip products, P_C, which is characterized by:*

$$J \times \left[\frac{W}{(1-v)z\theta P_C}\right]^{\frac{1}{\theta-1}} = S(W), \tag{5}$$

and

$$J \times z \left[\frac{W}{(1-v)z\theta(P_C)} \right]^{\frac{\theta}{\theta-1}} = \alpha_C I P^{\eta-1} P_C^{-\eta}, \text{ where } P^{1-\eta} = \alpha_C P_C^{1-\eta} + \alpha_O P_O^{1-\eta} \tag{6}$$

Equation (5) is derived from the labor market clearing condition, which states that the aggregate labor demanded by all J firms (LHS of Equation 5) must equal the total number of workers willing and able to supply labor at the equilibrium wage rate (RHS of Equation 5).

Equation (6) is based on the product market clearing condition, which states that the total production by domestic firms (LHS of Equation 6) must equal the demand of the representative consumer (RHS of Equation 6). This demand is negatively related to the price of chips and positively related to the overall price index P, which is a weighted average of the prices of chips and other products. Since the latter is supplied elastically at a price of P_O, we are left with two equations and two unknowns. We show that this system of equations yields a unique combination of equilibrium price and wage rate. Applying the implicit function theorem, we can then analyze the relationship between equilibrium employment and the intensity of protectionist policies.

Proposition 2. *Investment subsidies would increase equilibrium employment, whereas higher tariffs on raw materials or more stringent restrictions on labor access would lead to a monotonic decrease in equilibrium employment.*

Higher investment subsidies prompt firms to adopt more advanced technology, increasing the marginal revenue product and stimulating labor demand. However, if protectionist policies also increase the price of raw materials, this would partially offset the increase in the marginal revenue product of labor, creating an opposite effect. We refer to these two effects as

the "*firm demand channel,*" because they primarily influence the profitability of production for firms. When access to labor becomes restricted, the labor supply curve shifts inward, reducing the available workforce. As a result, firms must move up the supply curve to attract additional workers, leading to higher wages, higher production costs, and lower equilibrium quantities demanded. The overall impact of protectionist policies is thus uncertain ex-ante, as it depends on the relative strengths of the firm demand channel and the restricted labor access channel.

Proposition 3. *The stimulative effect of the firm demand channel will be dampened when the labor supply is less elastic. Meanwhile, the adverse effect of restricted labor access is amplified when the labor supply is less elastic and when the labor force relies more heavily on foreign workers.*

While Proposition 2 focuses on the direct effects (first-order derivatives) of protectionist policies, this analysis explores how these effects interact with labor market conditions (captured by the cross-derivative of firm production or employment with respect to protectionist policies and labor market conditions). Any stimulative impact through the demand channel encourages firms to invest in technology and improve production efficiency, thereby lowering the per-unit cost of chip products. As households increase their chip consumption, companies expand production, necessitating the hiring of more workers. This surge in labor demand drives up wages for chip workers, raising production costs for firms. When the labor supply is relatively inelastic, wage increases become more pronounced, pushing chip prices higher. These price increases partially counteract the initial cost reductions from efficiency improvements. Under such circumstances, the stimulative effects of the firm demand channel

are likely to be diminished.

On the other hand, increased restrictions on labor access force firms to raise wages to address the labor shortage created by these restrictions. This shortage is more severe when foreign workers make up a larger portion of the labor force. Furthermore, the wage increase becomes more pronounced when the labor supply is less elastic, leading to higher production costs and higher chip prices. These increased costs dampen demand, constrain production, and ultimately result in lower levels of equilibrium employment.

The results of Proposition 3 suggest that for two firms facing the same investment subsidy, input tariff, and labor access restrictions, employment will decline more for the one with a less elastic labor supply. Similarly, within the same firm, employment will decline more in the sector with a less elastic labor supply. These findings can be tested in a difference-in-differences regression framework, which compares employment changes across job categories within the same firm. In this setup, the direct effects of the protectionist policies are absorbed by firm fixed effects. However, the cross-elasticity results established in this proposition imply that employment is likely to decline more significantly for scientists and engineers—likely due to the specialized skills and challenging work conditions required, which limit the pool of eligible workers and contribute to an inelastic labor supply—relative to other professions within the same firm. The diff-in-diff results thus reflect the interactive effects of the firm demand and the labor restriction channels discussed above.

US Residents Versus Foreign Workers

Previously, we discussed the effect of protectionist policies on the equilibrium employment of US firms, discussing conditions under which the policies will lead to a decrease in firm

employment, especially employment in occupations with an inelastic labor supply (such as scientists and engineers). In this section, we delve deeper into firms' hiring strategies and analyze how these policies may lead to a change in the composition of workers, specifically between US residents and foreign workers with H-1B visas. We use d and h to denote the number of US residents and foreign workers hired by US manufacturers, which satisfy:

$$L = \left(\alpha_d^{\frac{1}{\rho}} d^{\frac{\rho-1}{\rho}} + \alpha_h^{\frac{1}{\rho}} h^{\frac{\rho-1}{\rho}} \right)^{\frac{\rho}{\rho-1}}, \tag{7}$$

where L represents total employment analyzed in the previous sections. We further model it as a CES aggregator of US residents and foreign workers, with α_d and α_h capturing their respective weights. These parameters may differ due to the unique skill sets of each group, which we will show empirically in Section C.2. This functional form is flexible, allowing these two groups of workers to act as complements or substitutes, depending on their skill sets.

In the extreme case where $\rho \to +\infty$, total employment becomes a linear combination of US and foreign workers, implying that the two types of labor are perfect substitutes. Under this condition, stricter labor access restrictions, such as reducing the H-1B quota, prompt firms to replace foreign workers with US residents. Consequently, while overall employment in US firms might decrease, the number of US residents employed could actually rise.

In contrast, in the other extreme where $\rho \to 0$, the production function is Leontief, implying that the two groups of workers are perfect complements. Restricting access to foreign workers reduces the hiring of both US residents and H-1B visa holders, as the complementary nature of the workforce makes one group essential to the productivity of the other.

In general, when US and foreign workers are more complementary in their skills and roles,

protectionist policies are more likely to result in simultaneous declines in the hiring of both US residents and foreign workers.

3 Sample Description and Summary Statistics

In this section, we present descriptive statistics for US chip manufacturing firms. Our primary data provider is Revelio Labs, which compiles and standardizes hundreds of millions of publicly available employment records to create the "world's first universal HR database," allowing users to track workforce dynamics and trends of any organization.[6] We also draw on data from LinkUp, USCIS, the Department of Education, and the Census Bureau (Fajgelbaum et al., 2020) to support different parts of our empirical analysis.

We gather and analyze information from millions of companies and nearly a billion employee profiles around the world to understand how the semiconductor industry's workforce is evolving, tracking everything from job trends to skills and educational levels. Our baseline panel organizes Revelio's raw data by firm, job category, and year, and we also disaggregate this panel by country. The job categories are defined by the Revelio clustering algorithm and consist of seven groups: Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist. We later expand this panel by adding finer job categories (e.g., design engineer vs. piping engineer) together with measures of seniority and prior experience. We further assemble supplementary datasets that map semiconductor skill distributions across countries and over time, track patent activity by chip manufacturers, and trace student cohorts acquiring chip manufacturing education. For brevity, we present descriptive statistics for our baseline panel of chip manufacturing firms below. Section B of the Appendix provides details on our

[6] Recent papers using the same data vendor include Amanzadeh et al. (2024), among others.

data collection, the resulting datasets, and summary statistics on supplementary datasets.

[Table 1 about here]

Panel A of Table 1 presents workforce dynamics across 68,949 firm-job category-year observations in the US semiconductor industry from 2014-2022. The data reveals substantial variation in employment levels, with logged employee counts ranging from near zero to nearly 5 (median 1.39, mean 1.76). Workforce activity is similarly diverse—while the median firm-job category experiences no hiring or separations in a given year, the 95th percentile shows considerable churn with hiring and separation rates reaching 83% and 50% respectively. On average, firms hire slightly more than they separate (16% vs 12% annually), indicating modest net growth. Panel B displays similar statistics for the US firms across their domestic and international segments. These statistics collectively provide information on hiring patterns and workforce dynamics within firms, highlighting the prevalence of experienced hires and general trends in employee turnover. Section C of the Appendix offers comprehensive insights into the global chip manufacturing talent landscape using Revelio's database of 1.6 million active employees worldwide with chip manufacturing skills as of March 2023.[7]

4 Baseline Specification

We estimate the average treatment effect of post-2018 US protectionism on science and engineering jobs at US semiconductor manufacturing firms by running the following difference-

[7]To assess Revelio's coverage, we compared its data with the Statistics of US Businesses (SUSB) Annual Data Tables for the five 6-digit NAICS codes relevant to our study (333242, 333994, 334413, 334418, 334515). In 2017, Revelio reported nearly 2,100 firms versus nearly 2,600 in the US Census, indicating substantial coverage of the US chip manufacturing sector and its employment counts.

in-differences regression:

$$y_{i,j,t} = \beta \text{Treated}_j \times \text{Post}_t + \alpha_{i,t} + \delta_{i,j} + \epsilon_{i,j,t}, \tag{8}$$

where i denotes the firm, j denotes the job category, and t represents the year. We focus on several key dependent variables $y_{i,j,t}$, which include the logarithm of the number of employees, hiring, separation, and turnover. We also examine rates of hiring, separation, net hiring, and turnover.

The variable $Treated_j$ is assigned a value of one for science and engineering job categories, and it is equal to zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years post-2018 and zero for the preceding years. The coefficient of interest in Equation (8) is β, associated with $Treated_j \times Post_t$. It estimates the homogeneous average treatment effect of US protectionism on science and engineering jobs at US chip manufacturing firms.

We incorporate firm-job category fixed effects $\delta_{i,j}$ and firm-year fixed effects $\alpha_{i,t}$. The former controls for fixed characteristics of firms' departments, recognizing that, for instance, some might naturally have large engineering/research or sales teams. Firm-year fixed effects allow for an intra-firm comparison of employment across various job categories, using non-engineering and non-scientist roles within the same year as counterfactual. For example, they allow us to compare the number of people working in Intel's science and engineering teams with the number of coworkers in Intel's sales, marketing, operations, and admin teams in the same year. Standard errors are corrected for clustering of observations at the firm

level.[8]

4.1 Main Findings on Employment

Table 2 reports our baseline estimates from the empirical specification in Equation (8). The coefficient on the treated-post interaction is negative and significant at the 1% level in all specifications in Panel A, with -0.03 for the log employment (Column 1), -0.09 for log hiring (Column 2), -0.04 for log separation (Column 3), and -0.09 for log turnover (Column 4). In other words, firms in the chip manufacturing industry experienced a significant decline in employment and hiring counts. They also experienced a similar decline in attrition, leading to a significantly smaller turnover of engineers and scientists starting in 2018.

[Table 2 about here]

Based on our findings shown in column (1) of Table 2's Panel A along with descriptive statistics from Appendix Figure B1, the US experiences a yearly loss of 2,285 science and engineering jobs ($3\% \times (66,382 + 9,768)$) in the chip manufacturing sector. From 2019 to 2022, during the post-treatment period, this amounts to a total reduction of 9,138 jobs in this industry. According to Figure B1, 67,793 engineers ($42,100 + 25,693$) and 9,784 scientists ($6,184 + 3,600$) graduate with undergraduate and master's degrees each year, positioning them as ideal candidates for these roles. While the decrease in job opportunities in the chip manufacturing industry doesn't necessarily imply these students will be unemployed, it does indicate a considerable reduction in their employment prospects within the chip manufacturing field.

[8] This method accounts for unobserved correlations within a firm due to changes in firm policies, fundamentals, or other factors that influence multiple job categories within the same firm simultaneously.

[**Figure 1 about here**]

Figure 1 provides evidence supporting the observable counterpart of the parallel trends assumption, which is essential for the difference-in-differences method we used in Table 2. It shows the time-specific treatment effects of protectionism on the number of science and engineering jobs at US chip manufacturers, revealing no discernible pre-trends. Post-treatment, the number of science and engineering jobs experiences a rapid and sustained decline.[9] The second panel separates trends for the treated and control groups, revealing strikingly parallel trajectories until 2018. After the onset of US protectionism, job numbers in the treated group decline by 4%, while the control group continues on its pre-existing path, showing a modest 1% increase over four years. This result is crucial for addressing the concern that estimated effects on science and engineering jobs are driven by growth in nontechnical roles—such as marketing or legal positions—within the control group.[10]

[**Figure 2 about here**]

Figure 2 presents additional evidence on effect dynamics for our main outcome variable—the log number of employees in science and engineering roles—using six different estimation strategies. These include Poisson pseudo-maximum likelihood (PPML) estimation with high-dimensional fixed effects (Correia et al., 2020), estimated with and without weights, as well as OLS and PPML regressions estimated with and without excluding the largest chip

[9] Figure B2 of the Appendix documents the effect dynamics associated with the remaining variables.

[10] The drop in employment in 2020 raises the possibility of COVID-19-related disruptions affecting the results. While it is plausible that the pandemic contributed to some of the observed decline, this is unlikely to fully explain our findings, including the ones on effect heterogeneity documented in Section 5. The parallel trends in employment up until 2018 indicate that the divergence began following the implementation of protectionist policies, aligning with the treatment effect. Moreover, the sharp decline in treated groups relative to control groups post-2018 suggests a policy-driven impact distinct from pandemic-related factors.

manufacturing firms based on their 2014 workforce size. Across all methods, the figure supports the parallel trends assumption in the pre-treatment period and shows consistent and statistically significant effects after treatment. Coefficient estimates are broadly similar, with overlapping confidence intervals across specifications.

Overall, these findings are consistent with our conceptual framework, demonstrating that protectionist policies can negatively impact the labor dynamics of US chip firms. Specifically, we find no significant change in employment growth for non-science and non-engineering roles but observe a sharp decline in science and engineering employment. This decline occurs when the reduction in labor supply caused by protectionist measures outweighs their stimulative effect on firm demand. Furthermore, a comparison of occupations within the same firm reveals that these policies, intended to promote production and employment, disproportionately harm workers in key roles in the US chip manufacturing sector. Through the lens of our model, this happens because these roles rely heavily on foreign labor and face an inelastic labor supply, likely due to the extensive training associated with these roles. Our model predicts that the most significant declines are likely to occur in these occupations.

4.2 Main Findings on Hiring and Attrition Rates

Next, we study the hiring and attrition rates, using a similar estimation method as in Panel A of Table 2. As shown in Panel B of Table 2, we see a significant post-2018 drop not only in the hiring rate but also in the attrition rate for engineers and scientists, compared to other job categories within the same firm-years. The coefficients are -0.03 and -0.01, both statistically significant at the 1% level. When we use the net hiring rate, we still see a statistically and economically significant coefficient of -0.02. In the last column, we present

results for the turnover rate, which once again leads to a negative and significant coefficient. All results provide strong evidence that both hiring and employee retention in these job categories declined with the start of the rise in US protectionism in 2018. Figure B3 shows how the effects evolve over time for Panel B variables and provides evidence supporting the parallel trends assumption. Figure B4 in the Appendix shows which engineering job categories were most affected by protectionism.[11]

Appendix Table B1 reports results from a more restrictive identification strategy that compares scientists and engineers across US and non-US operations within the same firm and year. This apples-to-apples comparison controls for firm-specific factors, technology needs, and skill requirements, isolating the geographic effects of US protectionist policies. The results remain robust: US technical employment declines relative to non-US counterparts, reinforcing that the main findings reflect true policy impacts rather than shifts in internal hiring composition.

4.3 Job Postings and Other Main Findings

We also examine job postings for scientist and engineering roles by merging LinkUp's job postings database with Revelio's job categories.[12] Using this data, Appendix Table B2 shows an increase in active job postings in the US for engineering and scientist roles, even after excluding software, IT, and data science jobs postings from our sample. This finding suggests

[11] Based on Revelio classifications, the largest effects are estimated for roles such as Stress Engineer (−22.76%) and Piping Designer (−16.61%). In un-tabulated analyses based on Revelio's role_k50 classification, we find the largest reductions in Scientist (−8.55%), IT Project Manager (−5.58%), and Mechanical Engineer (−4.80%) roles.

[12] LinkUp dataset, previously utilized in recent studies (Campello et al., 2020; Cohen et al., 2020; Gutiérrez et al., 2020), contains 250+ million records from nearly 60,000 company websites, covering public and private entities globally. Each entry includes job location, employer details, key dates, and O*NET occupation codes. We match O*NET occupation codes with Revelio's job categories using a linking table provided by Revelio.

that the decline in US scientists and engineers occurred despite continued hiring demand.

Our results so far reveal a decrease in science and engineering positions at US manufacturing firms following the start of US protectionism. Further analysis indicates that this reduction comes from fewer hirings rather than an increase in attrition; in fact, we find a decrease in turnover. These results are robust to the use of both logged employment counts and rates. Motivated by these findings, we next examine whether seniority or experience matter in the observed reduction in hiring.

Panel C of Table 2 highlights a significant decrease in first-job employees (with a coefficient of -0.03, significant at the 1% level) and a statistically insignificant and economically small decrease in the hiring of experienced personnel. In line with this finding, we also observe a 2% reduction in junior positions and no significant change in mid-senior positions. Appendix Figure B5 provides evidence on the dynamic effects along with trends for the treated and control units in the event time. It shows further evidence supporting the observable counterpart of the parallel-trend assumption. There is a significant drop in the job categories affected, which accounts for a substantial part of the observed changes. Overall, the figure highlights that companies are not just shifting to hire more newcomers in non-technical positions; rather, they're actually hiring fewer science and engineering staff after the beginning of the era of US protectionism.[13]

5 Mechanism and Effect Heterogeneity

In this section, we investigate the economic mechanisms driving our main findings through two complementary analyses. First, we compare workforce dynamics within the same firms

[13]Figure B6 of the Appendix presents our results on effect dynamics for the remaining Panel C variables.

across different geographic regions, contrasting US-based operations with their international counterparts to isolate the domestic effects of protectionist policies. Second, we examine how specific trade and immigration barriers—import tariffs, export tariffs, and H-1B visa restrictions—differentially affect US segments of chip manufacturers, testing whether these policy instruments explain the employment patterns we observe.

5.1 Estimating Effect Heterogeneity by Location

In this section, we examine how protectionist policies reshape the global workforce composition of US chip manufacturers. Using country-job category-year data, we investigate whether the engineer and scientist employment patterns documented in Section 4.1 reflect shifts in domestic hiring practices or broader changes in firms' international workforce allocation. To do so, we first run regressions on

$$y_{i,c,j,t} = \omega \text{Treated}_j \times \text{Post}_t \times \text{US}_c + \alpha_{i,t} + \pi_{c,t} + \rho_{j,t} + \delta_{i,c,j} + \epsilon_{i,c,j,t}, \tag{9}$$

where i denotes the firm, c denotes country, j denotes the job category, and t represents the year. Although the unit of observation is now at a finer level (as it includes the country), the dependent variables remain the same as those in Section 4. The coefficient of interest in Equation (9) is ω, associated with $\text{Treated}_j \times \text{Post}_t \times \text{US}_c$. It quantifies the average treatment effect of US protectionism on science and engineering jobs at US chip manufacturing firms within the US.[14]

Beyond capturing US-specific effects, Equation (9) offers a key advantage: it allows us to

[14] Goldberg and Pavcnik (2016) reviews how trade policy influences employment across different countries, highlighting the role of mobility frictions, industry affiliation, and local exposure, and summarizes key contributions in this literature.

control for job category–year level endogeneity, which was not feasible in Equation (8). In particular, $\rho_{j,t}$ accounts for shifts in the technology landscape or production processes that may lower demand for scientists and engineers while increasing demand for support roles.

5.1.1 Results on Global Workforce Dynamics of US Chip Manufacturers

Table 3 reports estimates from the specification in Equation (9). Panel A presents our key findings. The triple interaction term $\text{Treated}_j \times \text{Post}_t \times \text{US}_c$ reveals that US semiconductor companies significantly reduced their US employment (-5%, t-stat = 4.76). The decline in US employment stems from decreased hiring, which persists despite lower separation rates. These results are robust across various fixed effects specifications, including firm-country-job category, firm-year, country-year, and job category-year fixed effects.

[Table 3 about here]

Panel A reveals that protectionist policies significantly reduced employment of engineers and scientists at US chip manufacturers, with the effects concentrated domestically rather than reflecting broad industry decline. Post-2018, US-based employment fell substantially in technical roles while employment in foreign operations of these same firms showed minor increases. This divergent pattern suggests firms maintained their global workforce while specifically reducing domestic technical staff. Panel B confirms that these findings are robust when examining employment dynamics through rates rather than logged counts. Hiring, separation, net hiring, and turnover rates all declined significantly in the US following protectionist measures.

As illustrated in Figure 3, parallel pretreatment trends and sharp post-2018 divergence

provide strong evidence that protectionist policies prompted US chip manufacturers to fundamentally change their employment strategies. Rather than simply reducing overall technical capacity, firms appear to have strategically relocated technical talent away from US operations while preserving their global technical workforce. This reallocation suggests that companies adapt to policy constraints by maintaining innovation capabilities offshore while scaling back domestic technical employment.

[Figure 3 about here]

Panel C provides deeper insight into the compositional changes driving employment patterns, revealing that the modest growth in non-US employment reflects deliberate strategic workforce upgrading rather than simple headcount expansion. Specifically, there is a 3% increase in experienced workers taking junior and mid-senior positions overseas, suggesting that firms are systematically enhancing their international talent base by deploying experienced professionals (e.g., employees with OPT status that will need to switch to H-1B visas to continue working in the US) to roles abroad. This pattern likely reflects efforts to rapidly build technical capabilities at foreign operations, transfer institutional knowledge, or establish experienced leadership within international teams while maintaining cost advantages of overseas locations. The results in columns 5-8 of panel C provide an important corroboration of our main findings from Table 2, demonstrating that the employment effects are consistent in multiple model specifications and measurement approaches. This robustness is particularly valuable given the complexity of tracking employment changes across different geographies and seniority levels. Most notably, these results confirm a broader slowdown in non-managerial hiring that spans both entry-level recruitment and experienced worker

hiring. The consistency of these patterns across different analytical approaches strengthens confidence that protectionist policies fundamentally altered how chip manufacturers structure their global workforce, with firms adapting through strategic reallocation rather than proportional downsizing.

Table 3 employs trends in firms' non-US operations as additional counterfactuals to isolate the domestic effects of protectionist policies. This approach compares employment outcomes within the same firm and year across geographic segments—for example, contrasting Intel's scientist and engineer headcount in the United States versus its operations in countries like Canada and Mexico during the same fiscal period. By leveraging within-firm variation across locations, this design controls for company-specific factors and isolates the impact of US policy changes. We also conduct subsample analyses by individual countries to examine how protectionist measures differentially affected firms' employment decisions across specific international markets. The results of these analyses are shown in Figure B7 in the Appendix. As shown in this figure, US chip manufacturers significantly expanded their labor force in Canada, strategically amending its immigration policies to welcome more foreign engineers and scientists in 2017, as well as in several European countries including the Netherlands.[15]

5.2 Estimating Effect Heterogeneity by Tariff and Foreign Talent Exposures

Having established in the previous section that the employment effects documented in Section 4.1 are concentrated in US operations of chip manufacturers, we now turn to identifying the specific policy mechanisms driving these domestic changes. This section examines whether

[15] Esterline (2023) estimate the US lost 45,000 college graduates to Canada's high-skill visa (2017–2021). Among segments of US chip firms, 27.1% show a significant positive effect, 35.7% a positive but insignificant effect, 22.9% a negative but insignificant effect, and 14.3%—including the US—a significant negative effect.

the observed US employment patterns can be attributed to particular protectionist measures, focusing on the H-1B visa restrictions and tariff implementations that coincided with the broader policy shift. We investigate these channels by augmenting our triple difference framework from Equation (9) with additional interaction terms that isolate the effects of each policy instrument.

$$\begin{aligned} y_{i,c,j,t} = \phi_1 \, &\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i \\ &+ \phi_2 \, \text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{High Import Tariff}_k \\ &+ \phi_3 \, \text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{High Retaliation}_k \\ &+ \gamma \, \text{Treated}_j \times \text{Post}_t \times \text{US}_c \\ &+ \alpha_{i,t} + \pi_{c,t} + \rho_{j,t} + \delta_{i,c,j} + \epsilon_{i,c,j,t} \end{aligned} \tag{10}$$

In Equation (10), $Sponsor_i$ is an indicator that equals one if US chip manufacturer i filed at least one H-1B petition in fiscal year 2017, and zero otherwise. $High\ Import\ Tariff_k$ and $High\ Retaliation_k$ are equal to one for firms operating in NAICS code k with the highest exposure to import and retaliatory tariffs, respectively. To identify these industries, we use data from Fajgelbaum et al. (2020), who report US-imposed and retaliatory tariffs at the 10-digit HS code level. We compute average tariff rates by NAICS code as of 2018 following concordance tables from Pierce and Schott (2012).[16]

The coefficients of interest in Equation (10) are ϕ_1, ϕ_2, and ϕ_3, which estimate the impact of protectionist policies on science and engineering employment at US chip manufacturing firms that rely on foreign talent (as indicated by recent H-1B sponsorship) and on firms

[16]Section B.1.6 of the Appendix provides detailed information on our data collection process.

with NAICS codes that are more exposed to import and retaliatory tariffs. The coefficient γ captures the portion of the baseline effect ω, previously estimated in Equation (9), that is not explained by the heterogeneity in effects across the above dimensions. We report results based on specifications that also interact $\pi_{c,t}$ and $\rho_{j,t}$ with $Sponsor_i$, $High\ Import\ Tariff_k$, and $High\ Retaliation_k$. Our main findings remain robust when these controls are excluded.

5.2.1 Results on Tariff and Foreign Talent Exposures of US Chip Manufacturers

Table 4 presents evidence on how H-1B visa restrictions and trade barriers specifically affected US chip manufacturers using the framework in Equation (10). Panel A reveals that firms with a history of H-1B sponsorship experienced particularly severe employment disruptions in their US operations. These H-1B-dependent firms reduced hiring for science and engineering roles by 8% following the policy changes, consistent with visa restrictions constraining their access to international technical talent. The effects extend beyond hiring patterns: H-1B-sponsoring firms also reduced turnover by 6% and separations by 3%, indicating a shift toward aggressive worker retention strategies. This pattern suggests that when firms could no longer easily access foreign talent through H-1B visas, they responded by holding onto existing employees more tightly, likely reflecting the increased difficulty and cost of replacing technical workers under the new immigration restrictions.

[Table 4 about here]

Import tariffs also generate economically significant employment effects. Firms in industries with high exposure to import tariffs reduced their US-based science and engineering employment by 3% and cut turnover by 4%, suggesting that rising input costs and trade

uncertainty constrained firms' capacity to maintain and expand their domestic technical workforce. These reductions likely reflect the particular vulnerability of the technical roles involved in global production networks and supply chain coordination, where tariff-induced cost pressures and uncertainty in planning created the strongest incentives to reduce headcount. Panel B corroborates these patterns using employment rates rather than logged counts, confirming the robustness of our findings across different measurement approaches. Hiring rates declined by 2% at both H-1B-sponsoring firms and companies facing high import tariffs, while net hiring rates —a direct measure of workforce expansion— fell even more sharply. H-1B-dependent firms reduced net hiring by 3%, and firms in high-tariff industries cut net hiring by 2%. These substantial declines in net hiring rates reflect how both visa restrictions and trade barriers fundamentally altered firms' capacity to grow their domestic technical workforce, with the effects being particularly pronounced among firms most exposed to each policy channel.

Retaliatory tariffs, on the contrary, show weaker effects. This finding can be explained by two factors. First, while many US industries endured retaliatory tariff hikes (see, e.g., Morgan et al. (2022) and Autor et al. (2024) on retaliatory tariffs in agriculture), the chip sector remained effectively spared from large foreign retaliatory duties in the initial waves (Flaaen and Pierce, 2023). Second, retaliatory tariffs mainly trigger heightened uncertainty, a condition under which separations often become the main margin of adjustment (Davis and Haltiwanger, 1992; Amiti et al., 2019). Consistent with this, Panel B shows a 4% increase in separations.

Additional untabulated robustness checks using PPML regressions confirm our main findings. Chip manufacturers in industries facing the highest import tariffs show a 3% reduction

in their US science and engineering workforce, accompanied by substantial 10% declines in both hiring and turnover rates. Similarly, companies with recent H-1B sponsorship activity experience a 7% drop in US hiring. These results, which address potential concerns about the log-linear specification and zero-value observations in our employment data, provide reassuring evidence that our core findings are robust to alternative econometric approaches.

In summary, our findings in this section provide three important insights with broader implications for understanding protectionist policy effects. First, methodologically, the use of geographic variation within firms at the year-job category level enables more sophisticated identification strategies through stronger fixed-effect structures. This approach allows us to precisely isolate the impact of US protectionism on domestic science and engineering employment by controlling for unobserved firm characteristics, temporal shocks, and job category-specific trends that could otherwise confound our estimates.

Second, we document a striking pattern of strategic workforce reallocation in response to rising protectionism. Rather than simply downsizing, US chip manufacturers adapted by fundamentally restructuring their global operations: reducing domestic hiring while simultaneously expanding recruitment of experienced workers overseas for junior and mid-senior positions. This substitution strategy appears particularly pronounced in roles experiencing declining domestic interest, suggesting that firms proactively addressed skill shortages by relocating talent development activities abroad.

Third, our decomposition of policy channels reveals that both immigration restrictions and trade barriers generate substantial employment contractions through distinct but complementary mechanisms. H-1B visa limitations directly constrain firms' access to international technical talent, while import tariffs create cost pressures and uncertainty that reduce

firms' capacity to maintain domestic technical workforces. These effects are especially pronounced in science and engineering occupations, which face a relatively inelastic domestic labor supply and a historically high dependence on foreign workers, precisely the conditions our conceptual framework identifies as most vulnerable to protectionist interventions.

6 Effects of Protectionism on Chip-related Talent and Innovation

In this section, we examine how protectionist policies shape the chip-manufacturing talent pipeline by tracking educational cohorts over time and by immigration status. We then assess their impact on the US's share of the global workforce possessing chip-manufacturing skills, as well as their effects on innovation outcomes (e.g., patenting).

6.1 Decreasing Interest in Chip Manufacturing Education

Our unique dataset allows us to investigate whether the observed hiring declines in chip manufacturing stem from reduced student interest in semiconductor-related fields—i.e., supply-side shifts in student career preferences—, or do they reflect firms' constrained ability to hire despite sustained graduate interest—i.e., demand-side firm adjustments?

For this purpose, we focus on individuals who shared identical educational experiences with chip-skilled workers as of 2023: the same university, the same degree program, the same graduation year, and the same country. We then analyze their subsequent career choices between science and engineering positions versus other professional fields (e.g., finance, marketing, sales, or others), comparing patterns before and after 2018. This approach leverages educational peer groups as a natural comparison, controlling for program-specific factors

that might independently influence job market outcomes.

$$y_{c,d,j,t} = \tau \text{Treated}_j \times \text{Post}_t + \gamma_{c,d,j} + \theta_{c,t} + \zeta_{d,t} + \epsilon_{c,d,j,t}. \tag{11}$$

Our analysis focuses on $y_{c,d,j,t}$, a set of dependent variables capturing various labor market outcomes. Specifically, $\text{Log}(\text{Classmates}_{c,d,j,t})$ measures the number of individuals, sharing the same graduation country (c), degree type (d) from the same university, and year (t) alongside those with chip manufacturing skills as of 2023, entered job category j after graduation. We remove duplicate classmates to count each individual only once. $\text{Log}(\text{Salary}_{c,d,j,t})$, $\text{Seniority}_{c,d,j,t}$, and $\text{Log}(\text{Tenure}_{c,d,j,t})$ refer to the average salary, seniority level, and tenure duration of these classmates in their first jobs after graduation.

In specification (11), $Treated_j$ is assigned a value of one for science and engineering jobs, while it is equal to zero for finance, marketing, sales, operations, and administrative jobs. $Post_t$ takes a value of one for the years post-2018 and zero for the preceding years. The coefficient of interest is τ. This coefficient quantifies the homogeneous average treatment effect of protectionism on the number of science and engineering jobs taken by different educational cohorts—i.e., classmates of people with semiconductor skills—upon graduation.

To account for endogeneity, we incorporate a strong fixed effects structure. The country-degree-job category fixed effects ($\gamma_{c,d,j}$) help control for time-invariant factors that might simultaneously influence both educational choices and career outcomes within specific contexts, such as targeted government subsidies for particular technical fields or country-specific industry advantages. Country-year fixed effects ($\theta_{c,t}$) absorb annual shocks affecting all graduates within a country, including changes in visa policies, economic conditions, or labor

market regulations. Degree-year fixed effects ($\zeta_{d,t}$) capture temporal variations specific to educational programs, such as evolving curriculum standards, field-specific demand trends, or changes in graduate school admission policies. To account for correlation in unobserved factors within countries over time, we cluster standard errors at the country level.

Table 5 examines how protectionist policies affected the career outcomes of graduates who shared educational programs with chip manufacturing workers. We analyze four key dimensions of career trajectories: employment in science and engineering roles (Panel A), salary levels (Panel B), seniority progression (Panel C), and tenure in first jobs (Panel D). The analysis encompasses classmates from both undergraduate and graduate programs, providing comprehensive coverage of the technical talent pipeline that feeds into chip manufacturing and related industries.

[Table 5 about here]

The results reveal a significant shift in career patterns among educational peers of chip manufacturing workers after the onset of protectionist policies in 2018. Panel A demonstrates a consistent and substantial decrease in the number of classmates pursuing science and engineering careers, with coefficients negative and significant at the 1% level in all four specifications. The economic magnitude is large: we observe a 14-17% reduction in the logged number of classmates entering technical roles, suggesting that protectionist policies created spillover effects extending well beyond workers directly employed in chip manufacturing.[17]

Classmates who forgo science and engineering roles tend to shift into "control" sectors

[17]Effect dynamics can be found in Appendix Figure B8. At Carnegie Mellon, a source of technical talent for the chip sector, about 25% of seniors and 20% of juniors switch majors, with large outflows from mechanical engineering and electrical engineering (cornerstones of chip-manufacturing education). Career motives explain roughly 35% of these moves (Figures 5–6, https://bit.ly/4fq5rDN). The breadth of electives likely enables such changes (https://bit.ly/4lcQHtc).

such as finance, consulting, and marketing. Panels B and C show that graduates who do enter engineering or scientific positions receive higher starting salaries and advance slightly faster in seniority, while Panel D indicates no decline in first-job tenure. These patterns align with Neal (1999): heightened long-term career uncertainty can push students to change careers even when wages in their original fields rise.[18]

Appendix Section D.4 validates our findings using independent data from the US Department of Education on graduate cohorts, disaggregated by student residency status. We find that treated non-US residents experienced the most severe reductions, with degree completions falling by 17% for undergraduate programs and a dramatic 29% for postgraduate programs (see Table B3 of the Appendix). These declines likely reflect both reduced international student enrollment and increased difficulty for foreign students in securing post-graduation employment under tightened immigration policies. Perhaps most revealing is the differential impact on US residents across degree levels. While graduate degree completions by US students increased modestly by 5% (significant at the 10% level), undergraduate and pre-bachelor completions by US residents dropped significantly by 14% (significant at the 1% level). This divergent pattern suggests that protectionist policies may have encouraged some domestic students to pursue advanced degrees, possibly to enhance their competitiveness, while deterring others from entering technical fields at the undergraduate level.

Overall, this section provides strong evidence on two fundamental shifts in the post-2018 education landscape: substantial declines in both undergraduate and graduate cohort sizes among students in programs that historically produced chip manufacturing talent and a

[18]The numerical example based on Neal (1999) at `https://bit.ly/4l8FLfZ` shows that, under high uncertainty, moves to new careers rise and high firm- and industry-level wages that normally attract students to chip manufacturing (e.g., ϵ=4, θ=4) no longer suffice.

pronounced shift away from science and engineering careers toward alternative fields among students in programs providing chip manufacturing skills. These findings align with our conceptual framework, demonstrating that protectionist policies can generate counterintuitive outcomes. Rather than boosting domestic workforce, restrictions on foreign labor access can inadvertently reduce opportunities for US residents when the two groups possess complementary rather than substitutable skills in the production process.[19]

6.2 Changes in Skill Share

Do the employment reductions documented in previous sections translate into measurable shifts in the global distribution of chip manufacturing *skills*? In this section, we address this question directly by showing US's share of global chip manufacturing talent declined following the policy changes.

Table 6 quantifies this reallocation using country-year-skill level data, spanning 2019-2022, the only period for which skill data is available from the data vendor. We find a significant decline in the US share of global chip manufacturing skills following the onset of increased protectionism. Columns (1) and (2) show that chip-related skills in the US experienced a 5% reduction (significant at the 1% level) relative to other countries and skill categories in the post-2020 period. The year-by-year analysis in columns (3) and (4) shows that this decline was not a temporary adjustment and in fact intensified over time, with reductions of 3% in 2020, 6% in 2021, and 7% in 2022, all statistically significant at conventional levels.

[19]Additional analysis using Department of Education data on declared majors (results available upon request) corroborates these patterns, showing declines not only in degree completions but also in initial program enrollment, indicating that the effects begin early in students' academic careers and persist through graduation.

Figure 4 maps recent changes in each country's share of the worldwide chip manufacturing workforce. The US, shown in the lightest shade, experienced the largest decline in skill share globally, at 8.25%. Meanwhile, Canada and several other regions in Asia and parts of Europe, with more favorable policy environments or lower regulatory barriers, gained market share during this 2019-2022 period. These patterns indicate that protectionist policies not only reduced domestic employment at US chip manufacturers but also fundamentally altered US's position in the global semiconductor talent landscape.

[Table 6 and Figure 4 about here]

6.3 Patents

When chip manufacturers lose their engineers and scientists, does innovation suffer? In this section, we investigate whether employment constraints translated into measurable innovation losses by examining patent activity, the lifeblood of competitive advantage in the high-tech semiconductor industry.

Our analysis draws on Revelio's comprehensive patent database, tracking both the spark of innovation (patent filings) and its fruition (patent grants) across chip manufacturing firms from 2014-2022. We examine the number of patents filed to capture firms' immediate research productivity and the number of patents granted to measure successful innovation output two years later, as ideas need time to navigate the patent approval process. By focusing on firms that actively patent, we zero in on the industry's innovation leaders where policy effects should be most visible.

We find a significant decline in innovation by chip manufacturers following protectionist policies. Table 7 shows a 15% drop in patent filings by US chip manufacturing firms –

a statistically significant effect to the innovation pipeline. Even more concerning is that patent grants plummeted by 14-18%, indicating a significant drop in actual technological breakthroughs. Figure 5 presents changes over time after weighting observations by the inverse of firm age in 2014, revealing a stark difference in US patent activity before and after 2018. The decline in innovation output accelerated year after year, with 2022 patent filings declined by roughly 25% of pre-2018 levels. Importantly, the estimated effect was not distributed equally. Firms that historically tapped global talent through H-1B visas, as identified through 2017 USCIS records, drive the innovation shock. Patent filings by these companies drop by an additional 23% ($\approx 1 - e^{-0.27}$) beyond the baseline decline of 13% in the US.

[Table 7 and Figure 5 about here]

These findings paint an important picture: in attempting to protect US manufacturing, protectionist policies may have negatively impacted US innovation. The persistent nature of these declines suggests the damage extends far beyond immediate workforce disruptions, potentially undermining the technological foundations that keep US semiconductor firms competitive in global markets.

7 Robustness

In this section, we explore whether our results are robust across a comprehensive battery of alternative specifications and methodological approaches. In addition to what we include below, Appendix Section D presents additional key analyses: (i) comparing US scientists and engineers with their non-US counterparts within the same firm–year; (ii) controlling for

broader tech trends (data science and software); and (iii) examining domestic and international student degree completions using US Department of Education data.

7.1 Local Labor-Market Dynamics and Firm-Year Workforce Composition

Although firm × year fixed effects in our baseline specification absorb any shock common to all of a firm's operations in a given year, they cannot capture shocks that vary by location or by job category within the firm-year. Local downturns or booms might prompt chip manufacturers to cut engineers and scientists while increasing support staff, and firm-level changes in technology or production processes could shift demand away from technical roles. To show that our estimates remain robust even when allowing for both regional economic cycles and firms' yearly reallocation of employees across job categories, we introduce stronger control structures.

Panels A and B of Table 8 augment the baseline specification in Equation (8) with metropolitan area × year and firm × job category × metropolitan area fixed effects. Even after these controls, science and engineering categories in the post-2018 period show a 3% decline in log employment and a 9% drop in hiring (both significant at 1%), with separations and turnover also falling by 4% and 9%, respectively.

[Table 8 about here]

Panel C examines the global workforce dynamics of US manufacturers by reestimating Equation (9), further incorporating firm × metropolitan area × job category and job category × metropolitan area × year fixed effects. In doing so, we estimate a 5% reduction in employment and a 10% reduction in hiring in the US, alongside comparable declines in separations

and turnover. Collectively, Panels A, B, and C of Table 8 demonstrate that our main findings are not driven by regional economic cycles.

Panel D retains the Panel C sample and fixed effects and further includes firm × job category × year and firm × metropolitan area × year fixed effects. The estimates remain largely unchanged. In particular, we find a 3% reduction in the US science and engineering workforce driven by a 9% hiring decline, with separations and turnover down by 4% and 7%. These findings highlight that our main results are not driven by firm-year shifts in technology or production processes that might reduce demand for technical roles.

7.2 Poisson Pseudo-Maximum-Likelihood (PPML) Regressions

A potential concern with our log-linear specifications is that they may not adequately handle zero-valued observations or address distributional assumptions inherent in count data models. Employment counts, hiring events, and patent filings are inherently non-negative integer variables that may exhibit overdispersion or contain structural zeros, making Poisson-based estimators potentially more appropriate than OLS on logged outcomes (Cohn et al. (2022)).

To address these concerns, we re-estimate all our main specifications using Poisson Pseudo-Maximum-Likelihood (PPML) regressions with multiple levels of fixed effects, following the methodology of Correia et al. (2020). The PPML approach is particularly well-suited for our context because it can handle zero observations naturally without requiring the log(1+x) transformation, provides consistent estimates under weaker distributional assumptions, and has been shown to perform well with high-dimensional fixed effects.

Table 9 replicates our main employment findings, showing in Panel A that science and engineering positions experienced 5% declines in employment and hiring using PPML esti-

mation—effects that are statistically significant and economically similar to our OLS results. Panel C of the table further confirms the strong employment effects observed in US segments, consistent with earlier findings.[20]

Additionally, Appendix Table B4 demonstrates robustness when excluding the largest 10% of firms and presents both weighted and unweighted PPML specifications. For patenting outcomes, Appendix Table B5 shows even stronger effects under PPML estimation, with US firms experiencing 13-30% declines in patent filings and grants. Appendix Table B6 confirms our skill reallocation findings, with the US losing 4-5% of its global chip manufacturing skill share post-2018. Appendix Figure B9 presents event study plots based on PPML estimation for patent outcomes, corroborating the time-series patterns observed in our main analysis. The consistency of results across OLS and PPML specifications provides strong evidence that our findings are not artifacts of the estimation methodology but reflect genuine policy-induced changes in employment, innovation, and skill allocation patterns in the US semiconductor industry.

[Table 9 about here]

8 Conclusion

We document profound consequences of US protectionist policies on the chip manufacturing industry, particularly their impact on workforce dynamics, talent pipelines, innovation capacity, and global competitive positioning. Despite the stated goal of revitalizing domestic manufacturing, our findings demonstrate a significant decline in employment opportunities

[20] Our results are also robust to weighting by workforce size, which improves efficiency but can overscale between large and small firms.

for scientists and engineers, particularly in entry-level and junior roles. This contraction is driven by the interaction of restricted access to foreign labor and the industry's dependence on a global and interconnected supply chain.

We show that US chip manufacturing firms, constrained by protectionist measures, reduced domestic hiring while simultaneously increasing overseas recruitment, particularly in countries like Canada and the Netherlands that adopted more favorable immigration policies. Firms heavily reliant on H-1B visas experienced the sharpest declines in US-based employment, underscoring the critical role of foreign talent in maintaining innovation and operational capacity. The reduction in H-1B-sponsored positions further strained the industry's ability to attract and retain skilled workers, amplifying workforce shortages in critical technical roles.

Our analysis reveals that these workforce constraints translated into substantial innovation losses, with patent filings declining by 15% and patent grants falling by 14-18% at US chip manufacturers. H-1B-dependent firms faced even more severe innovation disruptions. These findings demonstrate that protectionist policies not only reduced employment but also fundamentally undermined the technological foundations that sustain competitive advantage in semiconductor manufacturing.

The geographic reallocation of expertise further illustrates the unintended consequences of these policies. Our skill share analysis shows that the US lost 5-7% of its global semiconductor talent concentration post-2018, with expertise migrating to countries with more favorable policy environments. This shift represents a structural change in the US's position within the global semiconductor talent landscape, suggesting that protectionist measures may have accelerated rather than reversed the offshoring of critical capabilities.

While our main specification focuses on the four years before and after 2018, our mechanisms have significant implications for longer-term effects. It is natural to assume that supply curves tend to flatten over time, which, in our context, suggests that the adverse impact of restricted labor access might diminish as the workforce gradually adapts to the new policy regime. However, our setting is unique in its focus on skilled labor. If workers foresee an outflow of foreign talent, they may be less motivated to join the field due to the lack of colleagues with complementary skills. This could lead to further declines in the number of prospective employees pursuing related degrees and majors. As a result, if skill complementarity exists among chip workers, an initial restriction on labor access could set off an amplification effect, causing a more prolonged and significant outflow in the long run.

Indeed, our findings highlight impacts that go beyond immediate workforce metrics to reveal fundamental shifts in educational and career trajectories. Using both self-reported LinkedIn data and official Department of Education records, we document substantial declines in chip manufacturing-related degree completions, with particularly severe effects on international students (17-29% reductions). Among graduates who do complete technical programs, we observe increasing migration toward alternative careers in finance, consulting, and other industries. This dual challenge poses long-term risks to the domestic talent pipeline and could undermine US leadership in semiconductor innovation.

Our findings have significant implications for the 2021 Facilitating American-Built Semiconductors (FABS) Act and the 2022 CHIPS and Science Act, which aim to bolster the US semiconductor industry through extensive investments to enhance US competitiveness globally. A report from the Semiconductor Industry Association (SIA) anticipates a significant expansion in the semiconductor workforce by 2030, with projections indicating a growth of

nearly 115,000 jobs.[21] They also estimate that around 60% of these new positions, predominantly technical roles, may remain unfilled based on current degree completion rates. Our estimates suggest that unless measures are taken to address the labor shortage by attracting and retaining domestic and international talent, the CHIPS Act may struggle to fully realize its objectives. Innovation losses and skill migration documented in our analysis indicate that successful industrial policy in sectors like chip manufacturing requires not only financial investment, but also supportive immigration and trade policies that enable access to global talent pools. Overcoming these challenges requires an approach that considers the combined effects of trade policies, immigration reforms, and educational investments.[22]

[21] See https://bit.ly/3SDPD5j. Other forecasts indicate a projected shortfall of 300,000 engineers and 90,000 technical workers in our country by 2030. See https://bit.ly/3OTd35B.

[22] See the 'Chipmaker's Visa' for H-1B program: https://bit.ly/49dum9E.

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Table 1. **Summary Statistics**

This table presents summary statistics for our key variables on US chip manufacturing firms and workforce from 2014 to 2022. In Panel A, *Log(Emp$_{i,j,t}$)* refers to the log of one plus the number of employees in job category j at firm i in year t. *Log(Hiring$_{i,j,t}$)*, *Log(Separation$_{i,j,t}$)*, and *Log(Turnover$_{i,j,t}$)* refer to the logs of one plus the numbers of new hires, separations, and turnover in job category j at company i in year t. New hires are employees whose first year at the firm is t, separations are those whose final year is t, and turnover equals the sum of new hires and separations. *Hiring Rate$_{i,j,t}$* (*Separation Rate$_{i,j,t}$*) is the ratio of new hires (separations) in job category j at company i in year t to that category's workforce in year $t-1$. *Net Hiring Rate$_{i,j,t}$* is the difference, and *Turnover Rate$_{i,j,t}$* is the sum, of *Hiring Rate$_{i,j,t}$* and *Separation Rate$_{i,j,t}$*. *Log(FirstJobEmp$_{i,j,t}$)* is the log of one plus the number of employees in job category j at company i whose first year of employment is t and who are hired without prior work experience. *Log(ExprEmp$_{i,j,t}$)* is the log of one plus the number of employees in job category j at company i whose first year of employment is t and who are hired with prior work experience. *Log(JunPosEmp$_{i,j,t}$)* is the log of one plus the number of employees hired in year t for roles with Revelio seniority levels 1–3 (i.e., trainee, junior, and associate levels) in job category j at company i. *Log(MidSenPosEmp$_{i,j,t}$)* is the log of one plus the number of employees hired in year t for roles with Revelio seniority levels 4–5 (i.e., manager and director levels) in job category j at company i. Panel B disaggregates Panel A variables by country, c.

Panel A: US Chip Manufacturer Workforce

	N	Mean	Median	SD	P5	P95
Log(Emp$_{i,j,t}$)	68,949	1.76	1.39	1.47	0.00	4.86
Log(Hiring$_{i,j,t}$)	68,949	0.62	0.00	0.96	0.00	2.89
Log(Separation$_{i,j,t}$)	68,949	0.59	0.00	0.92	0.00	2.77
Log(Turnover$_{i,j,t}$)	68,949	0.88	0.69	1.16	0.00	3.50
Hiring Rate$_{i,j,t}$	56,497	0.16	0.00	0.38	0.00	0.83
Separation Rate$_{i,j,t}$	56,497	0.12	0.00	0.22	0.00	0.50
Net Hiring Rate$_{i,j,t}$	56,497	0.04	0.00	0.38	-0.33	0.50
Turnover Rate$_{i,j,t}$	56,497	0.28	0.14	0.49	0.00	1.00
Log(FirstJobEmp$_{i,j,t}$)	68,949	0.95	0.69	1.23	0.00	3.50
Log(ExprEmp$_{i,j,t}$)	68,949	1.56	1.10	1.52	0.00	4.60
Log(JunPosEmp$_{i,j,t}$)	68,949	1.45	1.10	1.50	0.00	4.47
Log(MidSenPosEmp$_{i,j,t}$)	68,949	1.04	0.69	1.29	0.00	3.66

Panel B: Regional US Chip Manufacturer Workforce

	N	Mean	Median	SD	P5	P95
Log(Emp$_{i,c,j,t}$)	231,696	1.24	0.69	1.24	0.00	3.83
Log(Hiring$_{i,c,j,t}$)	231,696	0.36	0.00	0.72	0.00	2.08
Log(Separation$_{i,c,j,t}$)	231,696	0.33	0.00	0.67	0.00	1.79
Log(Turnover$_{i,c,j,t}$)	231,696	0.53	0.00	0.89	0.00	2.56
Hiring Rate$_{i,c,j,t}$	166,411	0.12	0.00	0.27	0.00	0.75
Separation Rate$_{i,c,j,t}$	166,411	0.10	0.00	0.22	0.00	0.50
Net Hiring Rate$_{i,c,j,t}$	166,411	0.01	0.00	0.29	-0.46	0.50
Turnover Rate$_{i,c,j,t}$	166,411	0.23	0.00	0.39	0.00	1.00
Log(FirstJobEmp$_{i,c,j,t}$)	231,696	0.60	0.00	0.86	0.00	2.40
Log(ExprEmp$_{i,c,j,t}$)	231,696	1.02	0.69	1.20	0.00	3.58
Log(JunPosEmp$_{i,c,j,t}$)	231,696	0.98	0.69	1.15	0.00	3.43
Log(MidSenPosEmp$_{i,c,j,t}$)	231,696	0.65	0.00	0.93	0.00	2.71

Table 2. **Science and Engineering Employment in US Chip Manufacturing Companies**

This table reports the estimated effects of protectionism on science and engineering employment in US chip manufacturing firms, based on the difference-in-differences approach outlined in Equation (8). Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data collection process. For all variables in Panel B, we set missing values to zero and control for these cases in regressions using an untabulated dummy variable. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.09***	-0.04***	-0.09***
	(-3.45)	(-8.93)	(-4.19)	(-7.73)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.975	0.874	0.863	0.889
Panel B: Analyses of Employment Growth				
	Hiring $\text{Rate}_{i,j,t}$	Separation $\text{Rate}_{i,j,t}$	Net Hiring $\text{Rate}_{i,j,t}$	Turnover $\text{Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.01***	-0.02***	-0.04***
	(-4.70)	(-3.54)	(-3.16)	(-5.16)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.393	0.390	0.342	0.421
Panel C: Analyses of Chip Manufacturing Workforce by Career Progression				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.01	-0.02**	-0.01
	(-4.27)	(-1.55)	(-2.04)	(-0.81)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.983	0.974	0.974	0.973

Table 3. **Protectionism and the Geography of Science and Engineering Employment**

This table reports the estimated effects of protectionism on science and engineering employment at US chip manufacturers, measured separately for jobs based in the US and in other countries. We use the difference-in-differences approach outlined in Equation (9). Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data collection process. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. US_c equals one if country c is the US, and zero otherwise. For all variables in Panel B, we set missing values to zero and control for these cases in regressions using an untabulated dummy variable. In Panel C, *FirstJobEmp*, *ExprEmp*, *JunPosEmp* and *MidSenPosEmp* are shortened to *First*, *Expr*, *Jun* and *MidSen* for brevity. The analysis spans the years 2014 to 2022. Standard errors are clustered two ways, by firm and country. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce (N=231,696)								
	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.05***	-0.07***	-0.04***	-0.07***	-0.05***	-0.07***	-0.04***	-0.06***
	(-4.76)	(-4.92)	(-3.23)	(-4.21)	(-4.74)	(-4.71)	(-3.12)	(-4.00)
$\text{Treated}_j \times \text{Post}_t$	0.02**	-0.03**	-0.01	-0.04**				
	(2.17)	(-2.39)	(-1.00)	(-2.28)				
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes
R-squared	0.948	0.781	0.760	0.806	0.948	0.781	0.760	0.807
Panel B: Analyses of Employment Growth (N=231,696)								
	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01***	-0.01***	-0.01**	-0.02***	-0.01***	-0.01**	-0.01**	-0.02***
	(-3.83)	(-2.68)	(-2.62)	(-3.88)	(-3.60)	(-2.64)	(-2.40)	(-3.72)
$\text{Treated}_j \times \text{Post}_t$	-0.01***	-0.00	-0.01**	-0.02***				
	(-4.03)	(-1.43)	(-2.62)	(-3.46)				
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes
R-squared	0.329	0.281	0.211	0.349	0.329	0.281	0.212	0.350
Panel C: Analyses of Chip Manufacturing Workforce by Career Progression (N=231,696)								
	$\text{Log(First}_{i,c,j,t})$	$\text{Log(Expr}_{i,c,j,t})$	$\text{Log(Jun}_{i,c,j,t})$	$\text{Log(MidSen}_{i,c,j,t})$	$\text{Log(First}_{i,c,j,t})$	$\text{Log(Expr}_{i,c,j,t})$	$\text{Log(Jun}_{i,c,j,t})$	$\text{Log(MidSen}_{i,c,j,t})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01***	-0.06***	-0.04***	-0.03***	-0.01***	-0.06***	-0.05***	-0.03***
	(-2.69)	(-4.90)	(-4.23)	(-3.15)	(-2.90)	(-4.88)	(-4.28)	(-3.15)
$\text{Treated}_j \times \text{Post}_t$	-0.01	0.03***	0.02**	0.02**				
	(-1.51)	(3.04)	(2.10)	(2.36)				
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes
R-squared	0.961	0.940	0.943	0.939	0.961	0.940	0.943	0.939

Table 4. **US Science and Engineering Employment After Trade and Labor Mobility Barriers**

This table presents our results on the heterogeneous effects of labor mobility barriers and tariffs on domestic science and engineering employment in US chip manufacturing firms, using the specification in Equation (10). Descriptions of all dependent variables are provided in the caption of Table 1, and Section B details the data collection process. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. US_c equals one if country c is the US, and zero otherwise. $Sponsor_i$ indicates whether firm i sponsored H-1B petitions in fiscal year 2017, based on USCIS's H-1B Employer Data Hub. $High\ Import\ Tariff_k$ ($High\ Retaliation_k$) equals one if industry k (6-digit NAICS) is the most exposed based on average import (retaliatory) tariffs, and zero otherwise. Tariff data are from Fajgelbaum et al. (2020) and explained in detail in Section B.1.6. Industry concordance follows Pierce and Schott (2012). For Panel B variables, missing values are set to zero and flagged with an untabulated dummy in regressions. Panel C shows the fixed effects included as controls. Standard errors are two-way clustered by firm and country. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce (N=231,696)				
	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.03	-0.08***	-0.03*	-0.06**
	(-1.43)	(-4.07)	(-1.71)	(-2.36)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{High Import Tariff}_k$	-0.03**	-0.02	-0.02	-0.04**
	(-2.16)	(-1.20)	(-1.14)	(-2.11)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{High Retaliation}_k$	-0.06	-0.03	0.01	-0.01
	(-0.99)	(-0.29)	(0.25)	(-0.08)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01	-0.03**	-0.00	-0.01
	(-0.89)	(-2.53)	(-0.32)	(-0.75)
R-squared	0.949	0.783	0.762	0.809
Panel B: Analyses of Employment Growth (N=231,696)				
	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.02**	0.01*	-0.03***	-0.01
	(-2.48)	(1.77)	(-4.01)	(-0.85)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{High Import Tariff}_k$	-0.02***	-0.01	-0.02**	-0.03***
	(-3.33)	(-1.58)	(-2.46)	(-3.31)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{High Retaliation}_k$	0.03	0.04**	-0.01	0.08
	(0.75)	(2.16)	(-0.33)	(1.52)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	0.01	-0.00	0.01	0.00
	(0.86)	(-1.19)	(1.41)	(0.11)
R-squared	0.334	0.302	0.231	0.372
Panel C: Controls for Panels A and B				
Firm FE × Country FE × Job Cat. FE	Yes	Yes	Yes	Yes
Firm FE × Year FE	Yes	Yes	Yes	Yes
$\text{Country FE} \times \text{Year FE} \times \text{Sponsor}_i$	Yes	Yes	Yes	Yes
$\text{Job Cat. FE} \times \text{Year FE} \times \text{Sponsor}_i$	Yes	Yes	Yes	Yes
$\text{Country FE} \times \text{Year FE} \times \text{High Import Tariff}_k$	Yes	Yes	Yes	Yes
$\text{Job Cat. FE} \times \text{Year FE} \times \text{High Import Tariff}_k$	Yes	Yes	Yes	Yes
$\text{Country FE} \times \text{Year FE} \times \text{High Retaliation}_k$	Yes	Yes	Yes	Yes
$\text{Job Cat. FE} \times \text{Year FE} \times \text{High Retaliation}_k$	Yes	Yes	Yes	Yes

Table 5. **Career Choices of Students Graduating with Chip Manufacturing Skills**

This table presents our results on the effects of protectionism on educational cohorts acquiring chip manufacturing education. We employ the specification in Equation (11). The sample consists of individuals who graduated in the same year, with the same degree, from the same university and country as those identified with chip manufacturing skills as of March 2023. Duplicate classmates are removed to ensure each individual is counted only once. *Log(Classmates$_{c,d,j,t}$)* is the natural log of the number of unique classmates who finished the same degree d from the same school in country c and year t with someone identified as chip-skilled as of March 2023 and are subsequently employed in job category j. *Log(Salary$_{c,d,j,t}$)* is the natural log of their average first-job salary, *Seniority$_{c,d,j,t}$* is the average first-job seniority level, and *Log(Tenure$_{c,d,j,t}$)* is the log of their mean first-job tenure. *Treated$_j$* is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. *Post$_t$* takes a value of one for the years after 2018 and zero for the preceding years. Section B of the Appendix offers detailed information on the data collection process. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Regressions of Log(Classmates$_{c,d,j,t}$)				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	-0.14***	-0.15***	-0.14***	-0.17***
	(-11.92)	(-13.61)	(-11.63)	(-14.10)
Observations	35,496	35,424	35,496	35,424
R-squared	0.940	0.950	0.945	0.956
Panel B: Regressions of Log(Salary$_{c,d,j,t}$)				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	0.03***	0.03***	0.04***	0.04***
	(3.05)	(3.06)	(3.48)	(3.51)
Observations	35,496	35,424	35,496	35,424
R-squared	0.994	0.995	0.994	0.995
Panel C: Regressions of Seniority$_{c,d,j,t}$				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	0.11***	0.10***	0.11***	0.11***
	(6.47)	(6.28)	(7.00)	(6.86)
Observations	35,496	35,424	35,496	35,424
R-squared	0.769	0.780	0.770	0.781
Panel D: Regressions of Log(Tenure$_{c,d,j,t}$)				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	0.02	0.02	0.02	0.00
	(1.59)	(1.14)	(0.98)	(0.25)
Observations	35,496	35,424	35,496	35,424
R-squared	0.943	0.946	0.943	0.947
Panel E: Controls for Panels A, B, C, and D				
	(1)	(2)	(3)	(4)
Country × Job Category × Degree FE	Yes	Yes	Yes	Yes
Year FE	Yes	No	No	No
Country × Year FE	No	Yes	No	Yes
Degree × Year FE	No	No	Yes	Yes

Table 6. **Cross-Country Composition of Skills in the Semiconductor Industry**

This table presents our findings on how US protectionism has influenced the geography of chip manufacturing skills. The sample is a country–year–skill panel drawn from Revelio's dynamic skills dataset, covering 245 countries and 75 skill categories. The analysis spans the years 2019–2022, the only period for which Revelio's dynamic skill data is available. Our main estimates (presented in column 2) are based on the following specification:

$$\textit{Log(Skill Stock}_{s,c,t}\textit{)} = \beta \text{Chip Skill}_s \times \text{US}_c \times \text{Post}_t + \mu_{c,s} + \eta_{c,t} + \gamma_{s,t} + \varepsilon_{s,c,t}.$$

Log(Skill Stock$_{s,c,t}$*)*, is the logarithm of the number of LinkedIn users in country c who list or are endorsed with skill s in year t, winsorized at the 1% tails. *Chip Skill*$_s$ equals one when the skill s belongs to the "electronics / semiconductors / design of experiments" category and zero otherwise. *US*$_c$ equals one if country c is the US and zero otherwise. *Post*$_t$ equals one for 2020–2022 and zero for 2019. Indicator variables $\mathbf{1}[\textit{Year} = t]$ take the value one in year t and zero in all other years. Section B of the Appendix offers detailed information on the data collection process. Standard errors are clustered at the skill category level. Statistical significance at the 1%, 5%, and 10% levels is denoted by $***$, $**$, and $*$, respectively.

	Log(Skill Stock$_{s,c,t}$)	Log(Skill Stock$_{s,c,t}$)	Log(Skill Stock$_{s,c,t}$)	Log(Skill Stock$_{s,c,t}$)
	(1)	(2)	(3)	(4)
Chip Skill$_s$ × US$_c$ × Post$_t$	-0.05**	-0.05**		
	(-2.40)	(-2.43)		
Chip Skill$_s$ × Post$_t$	0.01			
	(0.46)			
Chip Skill$_s$ × US$_c$ × **1**[Year=2020]			-0.03**	-0.03**
			(-2.39)	(-2.41)
Chip Skill$_s$ × US$_c$ × **1**[Year=2021]			-0.06**	-0.06**
			(-2.19)	(-2.21)
Chip Skill$_s$ × US$_c$ × **1**[Year=2022]			-0.07**	-0.07**
			(-2.51)	(-2.50)
Chip Skill$_s$ × **1**[Year=2020]			-0.00	
			(-0.25)	
Chip Skill$_s$ × **1**[Year=2021]			0.00	
			(0.06)	
Chip Skill$_s$ × **1**[Year=2022]			0.03	
			(0.98)	
Country FE x Skill Category FE	Yes	Yes	Yes	Yes
Country FE x Year FE	Yes	Yes	Yes	Yes
Skill Category FE x Year FE	No	Yes	No	Yes
Observations	70,247	70,247	70,247	70,247
R-squared	0.995	0.996	0.995	0.996

Table 7. **Patenting Activity in the Semiconductor Industry**

This table presents our findings on how US protectionism has influenced patenting activities of chip manufacturing firms. The sample is a firm–year panel (2014–2022) based on Revelio's "Assignee Matches" dataset. We retain firms that filed at least one patent during our sampling period. Our main estimates (presented in columns 1 and 4) are based on the following specification:

$$y_{i,t} = \beta \text{US Firm}_i \times \text{Post}_t + \mu_i + \gamma_{j,t} + \varepsilon_{i,t}.$$

Our dependent variables are defined as follows. *Log(Patents Filed$_{i,t}$)* and *Log(Patents Granted$_{i,t+2}$)*, are the natural logs of one plus the number of patents firm i files in year t and is granted in year t+2, respectively. *US Firm$_i$* is equal to one if firm i is a US firm based on PatentsView classification. *Post$_t$* takes a value of one for the years after 2018 and zero for the preceding years. *Sponsor$_i$* indicates whether firm i sponsored an H-1B petition in fiscal year 2017 based on the USCIS H-1B Employer Data Hub. All specifications include firm fixed effects (μ_i) and industry(6-digit NAICS)-by-year fixed effects ($\gamma_{j,t}$). Section B of the Appendix offers detailed information on the data collection process. Standard errors are clustered at the firm level, with $***$, $**$, and $*$ denoting significance at the 1 %, 5 %, and 10 % levels, respectively.

	Log(Patents Filed$_{i,t}$)			Log(Patents Granted$_{i,t+2}$)		
	(1)	(2)	(3)	(4)	(5)	(6)
US Firm$_i$ × Post$_t$	-0.15***		-0.11***	-0.18***		-0.14***
	(-6.67)		(-5.20)	(-7.55)		(-6.19)
Sponsor$_i$ × Post$_t$		-0.26***	0.11		-0.28***	0.03
		(-4.10)	(1.29)		(-4.31)	(0.42)
Sponsor$_i$ × US Firm$_i$ × Post$_t$			-0.35***			-0.27***
			(-3.22)			(-2.91)
Firm FE	Yes	Yes	Yes	Yes	Yes	Yes
Industry x Year FE	Yes	Yes	Yes	Yes	Yes	Yes
Observations	18,693	18,693	18,693	18,693	18,693	18,693
R-squared	0.878	0.878	0.879	0.885	0.884	0.885

Table 8. **Main Results After Controlling for Local Labor Market Dynamics and Yearly Changes in Firms' Workforce Composition**

This table presents our findings on the influence of protectionism on science and engineering employment in US chip manufacturing firms, controlling for local labor market dynamics and yearly changes in firms' workforce composition. Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data collection process. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. Panels A and B present results after controlling for firm × job category, firm × year, metropolitan area × year and firm × job category × metropolitan area fixed effects. Panel C controls for firm × country × job category, country × year, firm × metropolitan area × job category, and job category × metropolitan area × year fixed effects. Panel D retains all Panel C fixed effects and sample, and additionally includes firm × job category × year and firm × metropolitan area × year fixed effects. Metropolitan Area refers to the metropolitan area of the firm's headquarters (sourced from Revelio). Sections B.1 and B.2 provide detailed information on the data collection process and variable definitions. The analysis covers 2014–2022, with standard errors clustered by firm in Panels A and B, and two-way clustered by firm and country in Panels C and D. Significance at the 1%, 5%, and 10% levels is indicated by ***, **, and *, respectively.

Panel A: Analyses of Chip Manufacturing Workforce (N=67,950)				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.09***	-0.04***	-0.09***
	(-3.49)	(-8.82)	(-4.23)	(-7.73)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Metropolitan Area × Year FE	Yes	Yes	Yes	Yes
Firm × Job Category × Metropolitan Area FE	Yes	Yes	Yes	Yes
Panel B: Science and Engineering Employment by Career Progression (N=67,950)				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.02	-0.02**	-0.01
	(-4.22)	(-1.61)	(-2.10)	(-0.78)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Metropolitan Area × Year FE	Yes	Yes	Yes	Yes
Firm × Job Category × Metropolitan Area FE	Yes	Yes	Yes	Yes
Panel C: Analyses of US Workforce Dynamics (N=227,277)				
	$\text{Log}(\text{Emp}_{i,c,j,t})$	$\text{Log}(\text{Hiring}_{i,c,j,t})$	$\text{Log}(\text{Separation}_{i,c,j,t})$	$\text{Log}(\text{Turnover}_{i,c,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.05***	-0.10***	-0.05***	-0.10***
	(-4.50)	(-8.33)	(-5.00)	(-6.91)
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes
Firm × Metropolitan Area × Job Category FE	Yes	Yes	Yes	Yes
Job Category × Metropolitan Area × Year FE	Yes	Yes	Yes	Yes
Panel D: Additional Analyses of US Workforce Dynamics (N=191,151)				
	$\text{Log}(\text{Emp}_{i,c,j,t})$	$\text{Log}(\text{Hiring}_{i,c,j,t})$	$\text{Log}(\text{Separation}_{i,c,j,t})$	$\text{Log}(\text{Turnover}_{i,c,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.03***	-0.09***	-0.04***	-0.07***
	(-2.98)	(-7.08)	(-2.86)	(-4.55)
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes
Firm × Metropolitan Area × Job Category FE	Yes	Yes	Yes	Yes
Job Category × Metropolitan Area × Year FE	Yes	Yes	Yes	Yes
Firm × Job Category × Year FE	Yes	Yes	Yes	Yes
Firm × Metropolitan Area × Year FE	Yes	Yes	Yes	Yes

Table 9. **Main Findings Based on Poisson Pseudo-Maximum-Likelihood (PPML) Regressions**

This table reports the estimated effects of protectionism on science and engineering employment in US chip manufacturing firms, based on the main difference-in-difference specifications outlined in Equations (8) and (9). Our estimates are derived from a Poisson pseudo-likelihood regression with multiple levels of fixed effects (Correia et al., 2020). To ensure the mean and variance of the dependent variables are similar, we apply probability weights, calculated as the inverse of each firm's age in years as of 2014. Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data collection process. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. US_c equals one if country c is the US, and zero otherwise. The analysis covers 2014–2022, with standard errors clustered by firm in Panels A and B, and two-way clustered by firm and country in Panel C. Significance levels of 1%, 5%, and 10% are denoted by $\star\star\star$, $\star\star$, and $\star$, respectively.

Panel A: Analyses of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.05***	-0.05**	-0.03	-0.04**
	(-4.25)	(-2.12)	(-1.40)	(-2.20)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
Panel B: Science and Engineering Employment by Career Progression				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.04***	-0.04***	-0.05***	-0.04***
	(-3.57)	(-3.42)	(-3.86)	(-3.14)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
Panel C: Analyses of US Workforce Dynamics				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.03***	-0.06**	-0.09***	-0.07***
	(-4.23)	(-2.39)	(-3.53)	(-3.53)
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes
Job Category × Year FE	Yes	Yes	Yes	Yes
Observations	231,696	231,696	231,696	231,696

Figure 1. **Effect Dynamics: Science and Engineering Positions at US Chip Manufacturers**

The first figure shows the time-varying effects of protectionism on science and engineering employment in US chip-manufacturing firms. These effects are calculated using a difference in differences model as explained in specification (8). The second figure shows the evolution of the average logged number of employees for the treated and control groups, demeaned by year and treatment status. Section B of the Appendix offers detailed information on the data collection process and variable descriptions.

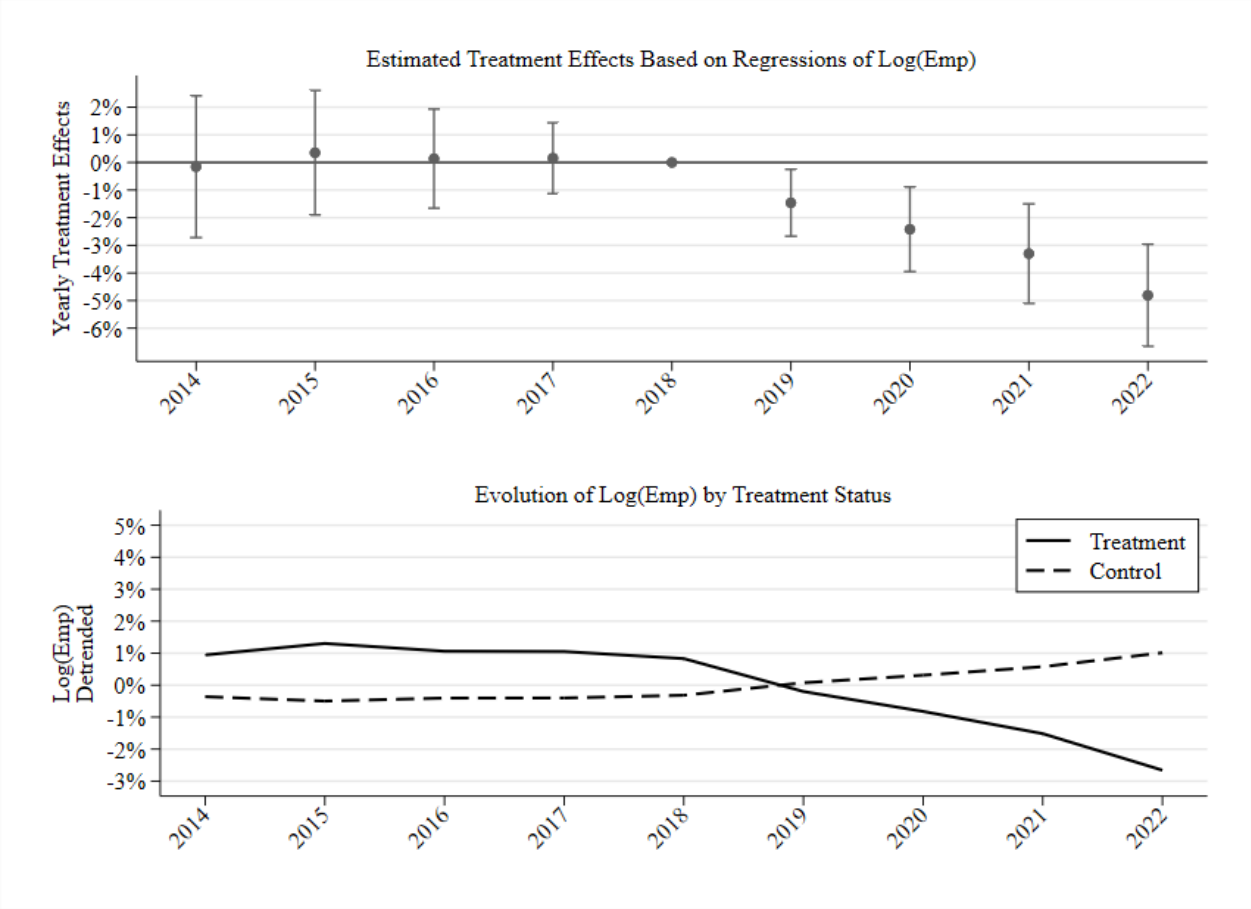


Figure 2. **Effect Dynamics: Alternative Estimation Methods**

This figure presents effect dynamics on the logged number of employees in science and engineering roles using different estimation methods and sample restrictions. All estimates are based on the difference-in-differences specification in Equation (8), with $\text{Log}(\text{Emp}_{i,j,t})$ as the dependent variable. The first estimation method (labeled as *Log1plus*) uses the specification as in Figure 1. The second one (labeled as *Poisson*) uses Poisson pseudo-likelihood estimation with high-dimensional fixed effects following Correia et al. (2020). The third applies the same Poisson estimation method, weighted by the inverse of firm age in 2014 (labeled as *Poisson (Wtd.)*). The fourth, fifth, and sixth replicate these three specifications after excluding the top 10% of firms by 2014 workforce size (denoted additionally as *Excl. Large Firms*). Standard errors are clustered at the firm level. The plot shows 95% confidence intervals. Section B of the Appendix offers detailed information on the data collection process.

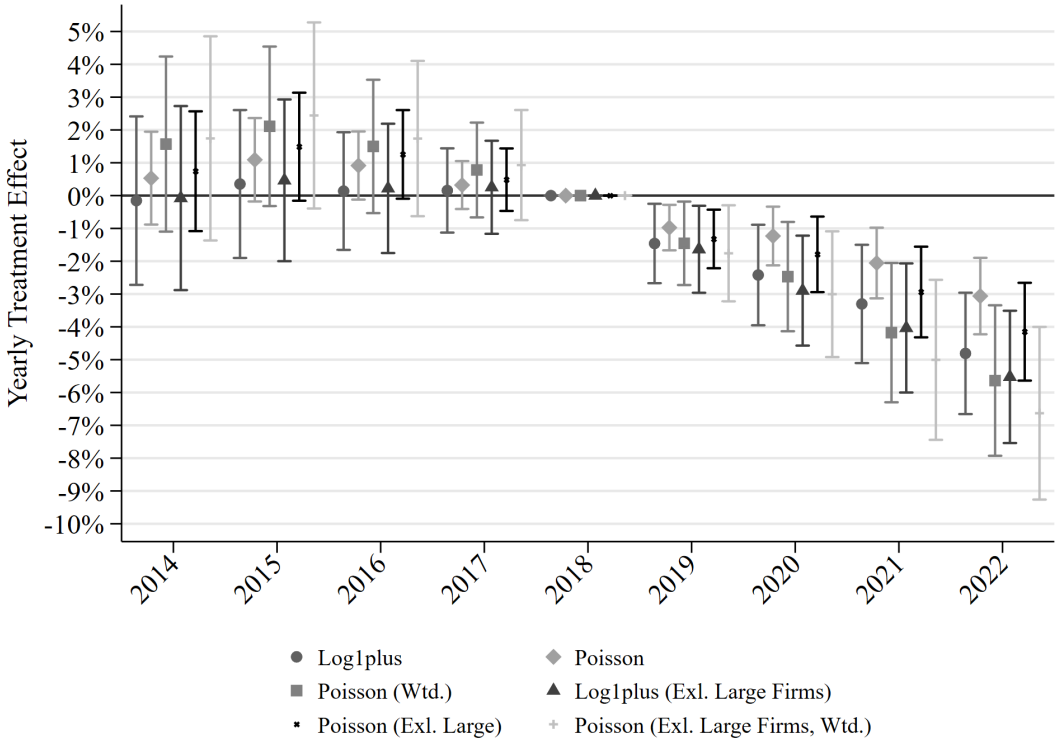


Figure 3. **Effect Dynamics: Science and Engineering Employment in the US vs. Abroad**

The figure illustrates effect dynamics on science and engineering employment, both within the US (represented by squares) and overseas (represented by triangles). This analysis is conducted using a difference-in-differences approach as outlined in specification (9), accounting for firm × country × job category fixed effects, as well as firm × year and country × year fixed effects. Each point estimate is shown with a 95% confidence interval, and standard errors are two-way clustered by firm and country. Section B of the Appendix offers detailed information on the data collection process.

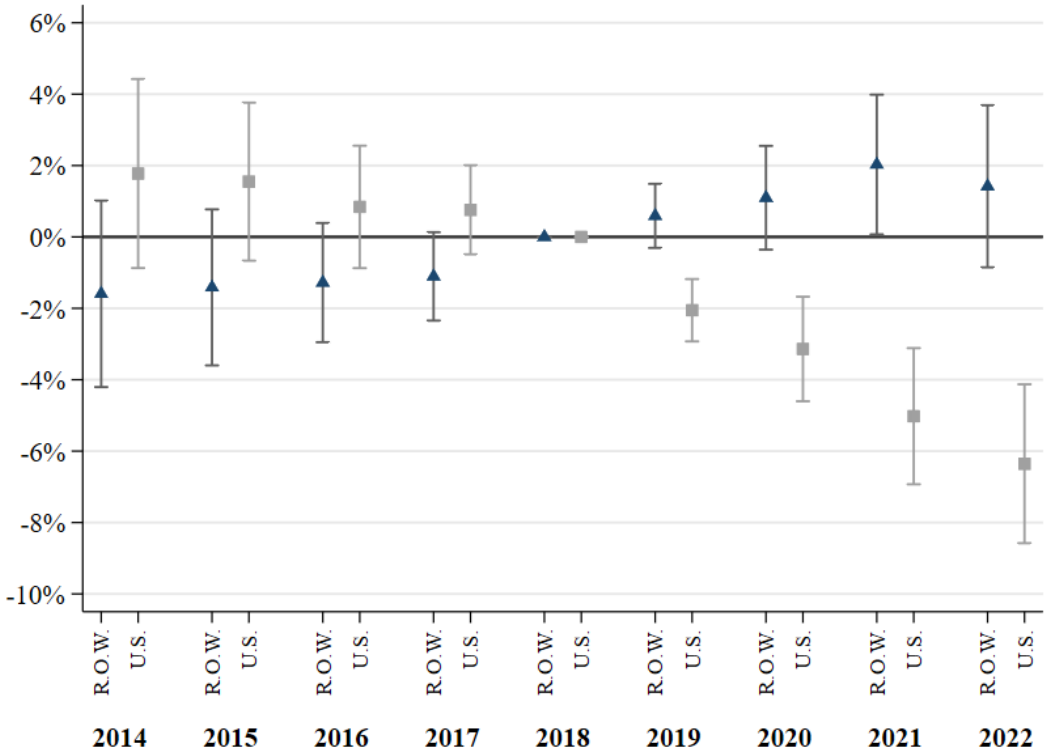


Figure 4. **Geographic Reallocation of Chip Manufacturing Skills**

This figure plots the change in each country's share of the global workforce possessing chip manufacturing skills from 2019 to 2022. The sample is a country–year–skill panel drawn from Revelio's dynamic skills dataset, which covers 245 countries and 75 skill categories. Revelio's dynamic skill data is available between 2019 and 2022. Chip skills are identified with Revelio's Skill 75 category, "electronics / semiconductors / design of experiments." For each year, we compute a country's chip-skill share by dividing the number of its LinkedIn users listing chip manufacturing skills on their profiles by the global count of such users in that same year. We then compute every country's 2022 share minus its 2019 share, and display the resulting differences in percentage points. We divide these differences into four bins, ranging from −8.25% (for the US) to 1.05% (for India), where darker shades indicating more positive values. Section B of the Appendix offers detailed information on the data collection process.

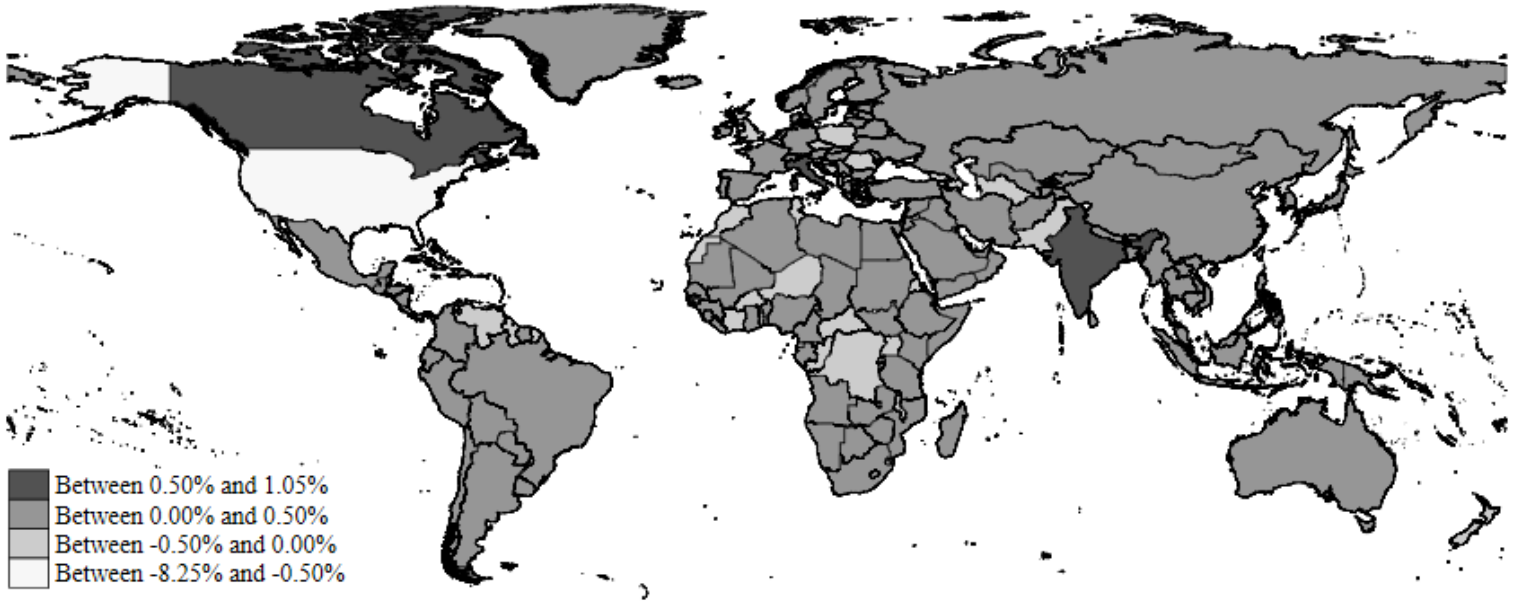
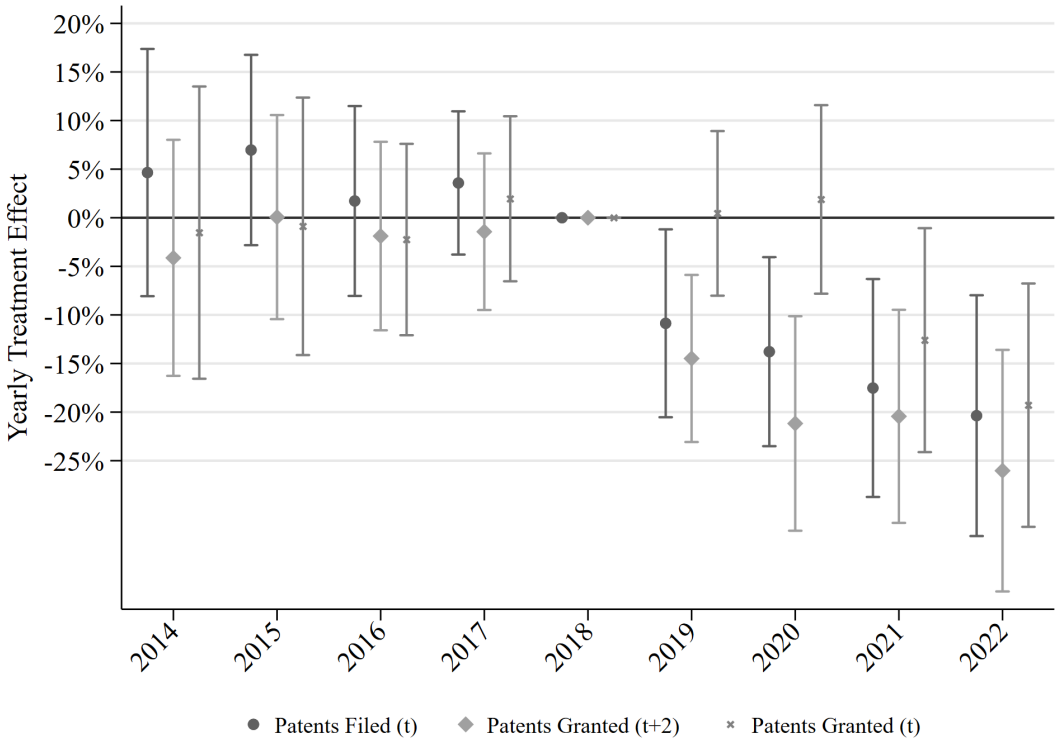


Figure 5. **Effect Dynamics: Protectionism and Patenting Outcomes**

This figure presents effect dynamics on patenting activities of US chip manufacturing firms. The effects are estimated using interactions between US Firm$_i$ and year dummies as in Section 6.3. The dependent variables are patent filings and granted patents within the same year, and patents granted two years later. Each point estimate is accompanied by a 95% confidence interval. The sample is a firm–year panel (2014–2022) based on Revelio's patent–firm-year "Assignee Matches" dataset. We retain firms that filed at least one patent during our sampling period. All regressions include firm fixed effects and industry × year fixed effects, with observations weighted by the inverse of firm age in 2014. Standard errors are clustered at the firm level, with $***$, $**$, and $*$ denoting significance at the 1 %, 5 %, and 10 % levels, respectively. Section B of the Appendix offers detailed information on the data collection process.



Internet Appendix for

When Protectionism Kills Talent

A Proof of Propositions

Proposition 1

Take the first-order conditions of the representative consumer's utility w.r.t chip and other products, and we have:

$$Y^{\frac{1}{\eta}}\alpha_C^{\frac{1}{\eta}}Y_C^{-\frac{1}{\eta}} = \lambda P_C \Rightarrow Y_C = (\lambda P_C)^{-\eta}\alpha_C Y \tag{A.1}$$

$$Y^{\frac{1}{\eta}}\alpha_O^{\frac{1}{\eta}}Y_O^{-\frac{1}{\eta}} = \lambda P_O \Rightarrow Y_O = (\lambda P_O)^{-\eta}\alpha_O Y, \tag{A.2}$$

where $Y \equiv \left(\alpha_C^{\frac{1}{\eta}}Y_C^{\frac{\eta-1}{\eta}} + \alpha_O^{\frac{1}{\eta}}Y_O^{\frac{\eta-1}{\eta}}\right)^{\frac{\eta}{\eta-1}}$, and λ is the Lagrange multiplier associated with the consumer's budget constraint. Substitute Equations (A.1) and (A.2) into the consumer's budget constraint (Equation 2), we have:

$$\begin{aligned} I &= P_O(\lambda P_O)^{-\eta}\alpha_O Y + P_C(\lambda P_C)^{-\eta}\alpha_C Y \\ &= \lambda^{-\eta}\left[P_O(1-\eta)\alpha_O + P_C(1-\eta)\alpha_C\right]Y \\ &= \lambda^{-\eta}P^{1-\eta}Y, \end{aligned} \tag{A.3}$$

where $P = \left[P_O^{1-\eta}\alpha_O + P_C^{1-\eta}\alpha_C\right]^{\frac{1}{1-\eta}}$ is the composite price index. Substitute Equation (A.3) into Equation (A.1), we get:

$$Y_C = I(P^{1-\eta}Y)^{-1}P_C^{-\eta}\alpha_C Y = \alpha_C I P^{\eta-1}P_C^{-\eta}. \tag{A.4}$$

Using the firm's first-order conditions in Equation (4), we can express firm j's labor demand as:

$$L = \left[\frac{W}{z(1-v)\theta P_C}\right]^{\frac{1}{\theta-1}}. \tag{A.5}$$

We have J symmetric firms in the economy, equating their total labor demand to the labor supply in the economy, we have the labor market clearing condition in Equation (5). Given firms' optimal labor demand, we can express the total output of domestic chip products as:

$$Y_C = Jy = JzL^{\theta} = Jz\left[\frac{W}{z(1-v)\theta P_C}\right]^{\frac{\theta}{\theta-1}}, \tag{A.6}$$

which we substitute into Equation (A.4) to obtain the product market clearing condition in Equation (6), which we reproduce below:

$$Jz\left[\frac{W}{z(1-v)\theta P_C}\right]^{\frac{\theta}{\theta-1}} = \alpha_C I P^{\eta-1} P_C^{-\eta}, \tag{A.7}$$

which we can rewrite into:

$$Jz^{\frac{1}{1-\theta}}\left(\frac{W}{\theta}\right)^{\frac{\theta}{\theta-1}} = \alpha_C I(1-v)^{\frac{\theta}{\theta-1}} P_C^{\frac{\theta}{\theta-1}} P^{\eta-1} P_C^{-\eta} = \alpha_C I(1-v)^{\frac{\theta}{\theta-1}} P_C^{\frac{1}{\theta-1}}\left(\frac{P}{P_C}\right)^{\eta-1}. \tag{A.8}$$

We can verify that the RHS of Equation (A.8) is strictly decreasing in P_C for all $\theta \in (0,1)$ and $\eta \geq 1$. Therefore, Equation (A.8) implies that the equilibrium wage rate W is a strictly increasing function of the domestic output price, P_C, and similarly, we can show that W is strictly increasing in z, and strictly decreasing in v. We can also verify these relationships using the Implicit Function Theorem by calculating:

$$\frac{\partial W}{\partial P_C} = \frac{W}{\theta P_C} + \frac{W(\theta-1)}{\theta}(1-\eta)\alpha_O\left(\frac{P_O}{P}\right)^{1-\eta} P_C^{-1} > 0 \tag{A.9}$$

$$\frac{\partial W}{\partial z} = \frac{W}{\theta z} > 0 \tag{A.10}$$

$$\frac{\partial W}{\partial v} = \frac{-W}{1-v} < 0. \tag{A.11}$$

Thus, we can write $W = w(P_C, z, v)$, with $\frac{\partial w(P_C,z,v)}{\partial P_C} > 0$, $\frac{\partial w(P_C,z,v)}{\partial z} > 0$, and $\frac{\partial w(P_C,z,v)}{\partial v} < 0$. In the subsequent analysis, we use w to denote the implicit function $W = w(P_C, z, v)$. We plug this relationship into the labor market clearing condition (Equation 5) to obtain:

$$\begin{aligned} J\left(\frac{\alpha_C I P^{\eta-1} P_C^{-\eta}}{Jz}\right)^{\frac{1}{\theta}} &= \lambda S\left[w(P_C, z, v)\right] \\ \Leftrightarrow A z^{\frac{-1}{\theta}} P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}} &= \lambda S\left[w(P_C, z, v)\right], \end{aligned} \tag{A.12}$$

where $A \equiv J(\frac{\alpha_C I}{J})^{\frac{1}{\theta}}$ is a constant. The LHS of Equation (A.12) is strictly decreasing in P_C, and the RHS is strictly increasing in P_C, implying a unique combination of product price and wage rate.

Proposition 2

We define the following based on Equation (A.12)

$$\Gamma \equiv A z^{\frac{-1}{\theta}} P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}} - \lambda S\left[w(P_C, z, v)\right] = 0. \tag{A.13}$$

Take the first order condition of Γ w.r.t the equilibrium product price, and protectionist policies, as represented by z, v, and λ, we have:

$$\frac{\partial \Gamma}{\partial P_C} = A z^{-\frac{1}{\theta}} \frac{\partial\left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} - \lambda \frac{\partial S}{\partial w}\frac{\partial w}{\partial P_C} < 0 \tag{A.14}$$

$$\frac{\partial \Gamma}{\partial z} = -\frac{1}{\theta} z^{-\frac{1}{\theta}-1} A\left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right] - \lambda \frac{\partial S}{\partial w}\frac{\partial w}{\partial z} < 0 \tag{A.15}$$

$$\frac{\partial \Gamma}{\partial v} = -\lambda \frac{\partial S}{\partial w}\frac{\partial w}{\partial v} > 0 \tag{A.16}$$

$$\frac{\partial \Gamma}{\partial \lambda} = -S < 0 \tag{A.17}$$

From the above equations, we can conclude that $\frac{\partial P_C}{\partial z} = -\left(\frac{\partial \Gamma}{\partial z}\right)\left(\frac{\partial \Gamma}{\partial P_C}\right)^{-1} < 0$. Similarly, we can show that $\frac{\partial P_C}{\partial \lambda} < 0$, and $\frac{\partial P_C}{\partial v} > 0$. Plugging this result back into the consumer's optimal demand Equation (A.1). We can conclude that the higher subsidy (larger z) increases firms' equilibrium production, while higher tariffs on raw materials (larger v) and tighter labor access restrictions (smaller λ) lower equilibrium output.

Proposition 3

We calculate the employment effect of greater subsidy, z, as follows:

$$\begin{aligned}
\frac{\partial \lambda S}{\partial z} &= \lambda \frac{\partial S}{\partial w} \times \left(\frac{\partial w}{\partial z} + \frac{\partial w}{\partial P_C} \times \frac{\partial P_C}{\partial z} \right) \\
&= \lambda \frac{\partial S}{\partial w} \times \left\{ \frac{\partial w}{\partial z} + \frac{\partial w}{\partial P_C} \times \left[-\left(\frac{\partial \Gamma}{\partial z} \right) \times \left(\frac{\partial \Gamma}{\partial P_C} \right)^{-1} \right] \right\} \\
&= \lambda \frac{\partial S}{\partial w} \times \left\{ \frac{w}{\theta z} + \frac{\partial w}{\partial P_C} \frac{\frac{1}{\theta} z^{-\frac{1}{\theta}-1} A P_C^{-\frac{1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}} + \lambda \frac{\partial S}{\partial w} \frac{w}{\theta z}}{z^{-\frac{1}{\theta}} A \frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}} \right]}{\partial P_C} - \lambda \frac{\partial S}{\partial w} \times \frac{\partial w}{\partial P_C}} \right\} \\
&= \lambda \frac{\partial S}{\partial w} \frac{w}{z\theta} \times \left\{ 1 + \frac{B + \lambda \frac{\partial w}{\partial P_C} \frac{\partial S}{\partial w}}{-C - \lambda \frac{\partial S}{\partial w} \frac{\partial w}{\partial P_C}} \right\} \\
&= \lambda \frac{\partial S}{\partial w} \frac{w}{z\theta} \times \left\{ \frac{C - B}{C + \lambda \frac{\partial S}{\partial w} \frac{\partial w}{\partial P_C}} \right\},
\end{aligned} \tag{A.18}$$

where we define:

$$\begin{aligned}
B &\equiv \frac{\partial w}{\partial P_C} \frac{1}{\theta} z^{-\frac{1}{\theta}-1} \frac{\theta z}{w} A \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C} \right)^{\frac{\eta-1}{\theta}} \right] > 0 \\
C &\equiv -z^{-\frac{1}{\theta}} A \frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C} \right)^{\frac{\eta-1}{\theta}} \right]}{\partial P_C} > 0.
\end{aligned}$$

Using Equation (A.9), we can verify that $B < C$. We also know that $\frac{\partial w}{\partial P_C} > 0$, which leads us to conclude that $\frac{\partial \lambda S}{\partial z}$ is strictly increasing in $\lambda \frac{\partial S}{\partial w}$. This implies that a labor market with a higher proportion of foreign workers (smaller λ) or a less elastic labor supply (smaller $\frac{\partial S}{\partial w}$)

would diminish the effect of stimulative subsidies.

Proposition 4

Finally, we examine the employment effect of more restrictive labor market protectionist policies. Note that the policy shifts the labor supply curve from $S(\cdot)$ to $\lambda S(\cdot)$, so $(1-\lambda)$ measures the intensity of the policy.

$$\begin{aligned}
\frac{\partial \lambda S}{\partial(1-\lambda)} &= -S - \lambda \frac{\partial S}{\partial w} \times \left(\frac{\partial w}{\partial P_C}\right) \times \left(\frac{\partial P_C}{\partial \lambda}\right) \\
&= -S - \lambda \frac{\partial S}{\partial w} \times \left(\frac{\partial w}{\partial P_C}\right) \times \left[-\left(\frac{\partial \Gamma}{\partial \lambda}\right) \times \left(\frac{\partial \Gamma}{\partial P_C}\right)^{-1}\right] \\
&= -S - \lambda \frac{\partial S}{\partial w} \times \left(\frac{\partial w}{\partial P_C}\right) \times \frac{S}{z^{-\frac{1}{\theta}} A \frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} - \lambda \frac{\partial S}{\partial w} \frac{\partial w}{\partial P_C}} \\
&= -S - \frac{S}{z^{-\frac{1}{\theta}} A \frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} \left[\lambda \frac{\partial S}{\partial w} \frac{\partial w}{\partial P_C}\right]^{-1} - 1} = -S - \frac{S}{D},
\end{aligned} \tag{A.19}$$

where we define:

$$D \equiv z^{-\frac{1}{\theta}} A \frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} \left[\lambda \frac{\partial S}{\partial w} \frac{\partial w}{\partial P_C}\right]^{-1} - 1 < -1. \tag{A.20}$$

Because $A > 0$ and $\frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} < 0$, it follows that $\frac{\partial \lambda S}{\partial(1-\lambda)}$ is increasing in $\lambda \frac{\partial S}{\partial w}$. This implies that a labor market with a higher proportion of foreign workers (smaller λ) or less elastic labor supply (smaller $\frac{\partial S}{\partial w}$) would exacerbate the negative impact of restricted labor access on equilibrium employment.

B Construction of Datasets and Variable Definitions

In this section, we describe our data sources, construction methods, and key variables. Section B.1 explains how we build five principal datasets from Revelio Labs: (i) a panel of labor force dynamics at US chip manufacturers; (ii) a panel of individuals with chip manufacturing skills as of March 2023; (iii) a dynamic skill dataset tracking the prevalence of skills by skill category, country and year; (iv) annual cohorts of students sharing educational affiliations with chip-skilled individuals that are identified based on the March 2023 scrape of Revelio data; and (v) firm-year level patenting activities of chip manufacturers. Section B.2 provides detailed definitions of the main variables used in our empirical analyses.

B.1 Methodology for Constructing Dataframes from Revelio Labs and Additional Descriptive Statistics

The data set used in our study comes from Revelio Labs, which specializes in providing individual-level granular employment data.[23] This data set includes extensive user-specific details, including current and past employment positions, educational background, names, skill sets, and demographic information, with a temporal benchmark of March 2023. We construct three principal dataframes for analysis: (i) the active labor force possessing chip manufacturing skills, (ii) the dynamics within the labor force of chip manufacturers, and (iii) annual cohorts of students who share educational affiliations with individuals skilled in chip manufacturing. Sections B.1.1 and B.1.4 below describe the methodology used to develop these dataframes, respectively. We also provide detailed descriptive statistics in each section to supplement the discussion in the main text.

[23] A detailed description of dataframes can be found on Revelio website: https://www.data-dictionary.reveliolabs.com/.

B.1.1 Labor Force Dynamics of US Chip Manufacturers

In our study, we delineate chip manufacturing firms using specific NAICS codes as the basis for classification. The initial step in our methodology involves processing the data from the company_ref dataframe, which entails iterating through rows to eliminate those lacking NAICS codes. Out of the 19,448,263 rows processed, 1,361,625 are retained, corresponding to firms identified by their NAICS codes, while 18,086,638 rows are discarded. The firms preserved in this filtered dataset are those associated with NAICS codes [334413, 334515, 334418, 333242, 333295, 333248, 333994], which are relevant to the chip manufacturing industry.

Subsequent to this filtration, we integrate this refined list of firms with data from position_file, which contains detailed information on individual employment positions. This integration aims to construct a person-firm-year panel, enabling a longitudinal study of employment patterns. To refine this panel further, we implement the following filters: we exclude records with undefined start dates (i.e., labeled as '\\N'), ensure that the start date precedes the end date, and remove entries where the country field is empty.

The transformation process then involves expanding each row of the dataframe to account for each year an individual held a position, thus adding a temporal dimension to the dataset. Consider, for example, a record which details the employment of an individual assigned user ID 301252435 and position ID 6893505588650110490 at "hohenloher spezialmöbelwerk schaffitzel gmbh" (identified by Revelio company ID 872817 and FactSet entity ID 08QGZ3-E), a German-based company. The tenure was extended from January 1, 2016, to March 1, 2023. In this period, the individual served as the "Assistent der Geschäftsleitung" (Assistant to the Executive Management), a role within the accounting and finance job category of the finance sector. Characterized by a high level of entry (seniority level 1), this position was offered an annual salary of €37,108.413. The data concerning this employment will be expanded into panel data covering the years 2016 to 2023.

We emphasize the use of annual panels over monthly panels to mitigate the introduction

of noise from inaccurately reported start dates on professional platforms like LinkedIn. This approach addresses the issue of 'false' turnover observed at the start and end of years, a common artifact when individuals do not specify the exact month of employment commencement or termination. Our methodological choice is validated by the close alignment of our yearly employment counts with those reported by LinkedIn, indicating the reliability of our data aggregation technique.

The final step in our analysis involves aggregating the unique number of individuals employed at each firm within a given year across different categories, thereby providing a comprehensive overview of employment trends in the chip manufacturing sector based on a person-firm-year panel. These aggregate data serve as the basis for our empirical analysis, offering insights into the dynamics of the labor market within this industry.

After transforming individual data into a person-firm-year panel format, we proceed to calculate the number of employees at each US manufacturing firm by job category (such as Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist) for each year, creating a detailed firm-job category-year dataset. From 2014 onwards, this dataset encompasses 5,436 distinct firms. To refine our analysis and exclude very small (micro) firms, and to ensure reliable counterfactual units (i.e., alternative job categories), we apply the following criteria: only firms that have been operational for at least three years by 2014, determined by the earliest LinkedIn profiles of their employees, are included. Additionally, we only consider firm-years that feature at least five job categories. This approach ensures the availability of at least three alternative job categories for scenarios where engineering and scientific positions are considered treated. Following these restrictions, the data set is reduced to 1,153 unique firms, resulting in 68,949 data points. To further enhance data quality, we apply winorization to all variables in the firm-job category year at the level of 2. 5% to eliminate outliers.

In the dataset related to firm-country-job category-year (referenced in Table 3 and described in Panel B of Table 1), we apply additional criteria to exclude 'phantom' segment

countries. These criteria involve removing countries that have data for fewer than 50 unique firms during the sampling period. Additionally, we exclude any firm-country-year group that contains fewer than two observations. This is to ensure that within a given year and country, firms are represented in at least two job categories.

B.1.2 The Active Labor Force Possessing Chip Manufacturing Skills

Our data collection process begins with identifying individuals with semiconductor skills within the Revelio dataset. This is achieved by filtering the skill_file dataset to include only those entries where the 'skill_k75' variable—Revelio's proprietary method for clustering skills reported by individuals or their connections—equals "electronics / semiconductors / design of experiments." This category encompasses a broad spectrum of skills related to the semiconductor field, including electronics, circuit design, semiconductor fabrication, and integrated circuit design, among others. Specifically, these skills are: *logic design, circuit design, pcb design, soc, semiconductors, verilog, ic, asic, digital electronics, vhdl, doe (design of experiments), metrology, failure analysis, power supplies, semiconductor industry, integrated circuits (ic), thin films, silicon, analog, electro-mechanical, hardware development, embedded c, fpga, cadence, vlsi, ni multisim, microcontrollers, power electronics, connectors, tcl, xilinx, digital signal processors, proteus, rtl coding, xilinx ise, orcad, field-programmable gate arrays (fpga), rtl design, altera, product engineering, mplab, pspice, autosar, pcie, schematic capture, mixed signal, analog circuit design, signal integrity, x86, synopsys tools, semiconductor fabrication, cadence virtuoso, intel, photolithography, mems, ncsim, modelsim, electronics, formal verification, systemverilog, integrated circuit design, functional verification, hardware architecture, multisim, microelectronics, microprocessors, microchip pic, vacuum, electronic engineering, computer architecture, processors, electrical machines, 8051 microcontroller, pcb layout design, application-specific integrated circuits (asic), system on a chip (soc), circuit analysis, keil, logic synthesis, cst microwave studio, hardware design, agilent ads, pll, cmos, power management, hfss, eda, embedded software programming, sputtering, semiconductor*

process, electronics hardware design, physical verification, can, tcl-tk, fpga prototyping, pvd, process integration, cvd, plasma etch, pecvd, computer engineering, spice, orcad capture cis, physical design, low-power design, arm cortex-m, very-large-scale integration, canoe, static timing analysis, dft, dsp, drc, semiconductor device, device characterization, cadence spectre, analog circuits, timing closure, ltspice, can bus, digital circuit design, very-large-scale integration (vlsi), electronic circuit design, yield, uvm, field-programmable gate arrays, system verilog, inverters, serdes, compilers, gage r&r, primetime, systemc, embedded c++, flash memory, semiconductor manufacturing, integrated circuits, application-specific integrated circuits, system on a chip.

Given the repetition in a few skill labels, such as 'integrated circuits appearing in various forms, we later consolidate similar skills into unified categories for clarity. Using these refined data, we construct a dataframe centered on Revelio's unique individual identifiers. This dataframe includes dummy variables for each skill, indicating whether an individual possesses that particular skill. For instance, if an individual has listed only 'orcad capture cis' as their skill, then all dummy variables except for 'orcad capture cis' will be set to zero, while the dummy for 'orcad capture cis' will be marked as one. This methodical approach enables us to systematically categorize and analyze the semiconductor skills present within the dataset.

We then merge the above dataframe with position_file, which contains the individual level position data, and company_ref, which contains static firm data. We remove rows lacking 'naics_code' data (0.09% of the firms), which are essential for mapping into two- and six-digit NAICS codes. The resulting data set comprises records of job positions held by individuals identified by their chip manufacturing skills, indicated through dummy variables. To isolate active employees within this dataset, we apply filters to select only those whose positions were active as of March 1, 2023, and whose records include a valid name for the ultimate parent company. Additionally, we exclude records where the country field is marked as 'empty'.

In this refined dataset, we determine the distinct number of individuals according to country, firm, and industry. When conducting analyses at the firm level, which involve categorizing employees based on their seniority, we adopt two key strategies: positions missing seniority information are omitted and we set guidelines for handling cases where an individual holds more than one position simultaneously. For instance, should an individual be documented as having concurrent employment (such as an academic with a role at Penn State University and another at Intel within the same period), we exclusively retain the position that ranks higher in seniority. This method ensures the accuracy of our data by eliminating the potential for missing data and double-counting individuals.

In the context of employment within US government entities, our analysis identifies significant numbers of individuals working for various departments and agencies, showcasing the breadth of employment within this sector. Notable employers include the United States Navy, the United States Air Force, the United States Army, Sandia National Laboratories, Jet Propulsion Laboratory, the Federal Aviation Administration, the United States Department of Defense, Lawrence Livermore National Laboratory, National Aeronautics & Space Administration, and the United States Marine Corps.

B.1.3 Dynamic Chip Manufacturing Skill Data

In addition to the skill data we construct from raw Revelio records, we also rely on dynamic skill data that we cannot compile ourselves, as Revelio's raw skill data are static. To address this, we request from Revelio their historical scrapes of skill information over time. Revelio informs us that dynamic skill data are only available starting in 2019. From this dataset, we obtain the number of employees—identified by unique individual identifiers as described in Section B.1.2—from each country who report having a given skill in each year.

In this dataset, Revelio maps the raw skill entries into 75 broader skill categories by country and year. LinkedIn allows up to 100 skills to be added to each profile. The skill mapping table evolves over time, but Revelio uses a consistent version of their linking table

that accounts for this variation. The final dataset therefore contains, for each country-year-skill combination, the number of employees in Revelio's database who possess that skill. Skills may be reported directly by individuals on their LinkedIn profiles—e.g., to improve job market visibility, similar to how a professor might list publications on a CV—or added through peer endorsements that the individuals choose to accept.

B.1.4 Annual Cohorts of Students Who Share Educational Affiliations With Individuals Skilled in Chip Manufacturing

We also construct a dataset focusing on the classmates of individuals possessing chip manufacturing skills, drawing on various data sources provided by Revelio. This data set is formulated by initially creating a data frame of individuals with chip manufacturing experience, as detailed in Section B.1.2, with the notable distinction that our selection does not limit itself to individuals currently employed. We begin by filtering for the latest educational degrees of these individuals using the education_file. With this filtered data, we further analyze the education_file to pinpoint individuals who graduated from the same school and program in the same year. During this process, we apply stringent filters to ensure data quality, excluding rows where details such as 'school', 'enddate', 'field_raw', and 'degree' are either not provided, marked as "\N", or labeled as "empty". After these exclusions, we only keep those rows with valid 'enddate'.

To identify a person's classmates accurately, we apply criteria ensuring they share the same 'school', 'degree', and 'field_raw', and have graduated in the same year. This methodological approach allows us to comprehensively map out the educational networks surrounding individuals skilled in semiconductor manufacturing. Subsequently, we explore the position_file, which contains data on the jobs the classmates take after their graduation. We impose certain restrictions on the initial positions these classmates take after graduating from the same programs as the people with chip manufacturing skills. This includes keeping jobs that are acquired only after graduation date, focusing on positions obtained within two

years of graduating, prioritizing the first job started if multiple jobs are taken simultaneously, and excluding jobs without specified 'country' data. We also drop classmates from high schools and associate degree programs. Through these filters, we compile data reflecting the employment characteristics of the classmates of individuals with chip manufacturing skills. Importantly, to prevent double counting, we count the number of unique ID numbers associated with individuals, thereby avoiding the duplication of counts for classmates possessing chip manufacturing skills within a specific year.

B.1.5 Data on Chip Manufacturing Patents

We also use novel patent data ("Assignee Matches") for US chip manufacturing firms based on a linking table created by Revelio Labs. The dataset connects patent records from the US Patent and Trademark Office (USPTO), accessed through PatentsView, to firm identifiers (RCIDs) in Revelio's database. For assignee matches, each `patent_id` and `assignee_sequence` combination in the PatentsView data is matched to an RCID based on Revelio's proprietary company mapping model. The matches are unique at the `(patent_id, assignee_sequence)` level and include only assignees that are organizations, not individuals.

For each matched patent, the dataset includes key information such as the filing date, grant date, title, and type of assignee. It also provides standardized firm names and identifiers that can be merged with Revelio's employment data. This allows us to track patenting activity by firm and link it to workforce changes over time.

We use this dataset to construct yearly measures of innovation at the firm level, including the number of patents filed and the number granted. Because patents are often granted with a delay, we also count the number of patents granted after two years of filing. This is useful because it captures innovation activity that occurs just after our sample period ends in 2022, and these outcomes help predict firm dynamics in the following years.

B.1.6 Data on Tariff Exposure

To explore the influence of tariffs on science and engineering jobs within the chip industry, we employ data on tariffs from Fajgelbaum et al. (2020), who report US-imposed tariffs on foreign countries at the 10-digit HS code level along with retaliatory tariffs. Our first step involves calculating the average scaled tariff rates by the HS-10 code and year. Our primary analysis focuses on tariffs as of 2018, considering that the post-2018 period is the post-treatment period in our analyses.

To calculate import and retaliatory tariff exposures, we use the concordance tables from Pierce and Schott (2012), which map NAICS codes to HS-10 codes. This mapping introduces useful industry-year variation, as different NAICS codes face different levels of tariff exposure. Using this variation, we classify industries into high and low tariff exposure groups. Specifically, we define the high-exposure import or retaliatory tariff group as the single industry with the highest average import or retaliatory tariff, while all other industries serve as the control group.

NAICS code 334413 falls into the high import tariff exposure group, with an average scaled import tariff of 13.18%. This industry is subject to 45 distinct tariffs, compared to only 14 for NAICS code 333242. Tariff exposure also varies in intensity: for example, NAICS code 334413 has a maximum average tariff of 24.4% across matched HS-10 codes and countries in 2018, while NAICS code 334418 faces a maximum of 17.9% and an average of 8.31%. On the retaliation side, NAICS code 333994 represents the high retaliatory tariff exposure group.

B.2 Variable Definitions

This section provides detailed descriptions of the variables used in our study. The variables presented in Panel B of Table 1 correspond to those introduced in Panel A, yet they are analyzed at a more granular level, encompassing firm, country, job category, and year. For the sake of conciseness, their descriptions are not repeated here.

- **Log(Emp$_{i,j,t}$):** The natural logarithm of the sum of one and the total number of employees in job category j at company i in year t.

- **Log(Hiring$_{i,j,t}$):** The natural logarithm of the sum of one and the number of new hires in job category j at company i in year t. New hires are employees whose initial year of work at the firm begins is year t.

- **Log(Separation$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees in job category j leaving company i in year t. Leaving the company refers to the employees for whom year t marks the final year of their employment at the firm.

- **Log(Turnover$_{i,j,t}$):** The natural logarithm of the sum of one and the total of new hires and leaving employees in job category j at company i in year t.

- **Hiring Rate$_{i,j,t}$:** The ratio of the number of new hires in job category j at company i in year t to the total number of employees in the same job category at the company in the previous year $(t-1)$.

- **Separation Rate$_{i,j,t}$:** The ratio of the number of employees leaving in job category j at company i in year t to the total number of employees in the same job category at the company in the previous year $(t-1)$.

- **Net Hiring Rate$_{i,j,t}$:** The difference between the hiring rate and the separation rate for job category j at company i in year t.

- **Turnover Rate$_{i,j,t}$:** The sum of the hiring rate and the separation rate for job category j at company i in year t.

- **Log(FirstJobEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees in job category j at company i whose first year of employment is t and who are newly hired without prior work experience.

- **Log(ExprEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees in job category j at company i who are hired in year t with previous work experience.

- **Log(JunPosEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees hired in year t for junior positions (seniority levels 1 to 3) in job category j at company i.

- **Log(MidSenPosEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees hired in year t for mid-senior positions (seniority levels 4 and 5) in job category j at company i.

- **Log((Classmates$_{c,d,j,t}$)**: This is the logged number of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

- **Seniority:** Defined as an ordinal variable between 1 and 7: 1. Entry Level (e.g., Software Engineer Trainee); 2. Junior Level (e.g., Junior Software QA Engineer); 3. Associate Level (e.g., Lead Electrical Engineer); 4. Manager Level (e.g., Superintendent Engineer); 5. Director Level (e.g., VP Network Engineering); 6. Executive Level (e.g., Director of Engineering, Backend Systems); 7. Senior Executive Level (e.g.,CFO; CEO)

- **Log(Avg. Salary$_{c,d,j,t}$)** : This is the average first-job salaries of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

- **Avg. Seniority$_{c,d,j,t}$** : This is the average first-job seniority levels of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

- **Log(Tenure$_{c,d,j,t}$)**: This is the average first-job tenures of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

C Detailed Landscape of the Global Chip Manufacturing Talent

The United States (Texas Instruments, Fairchild Manufacturing, and Intel) led chip manufacturing until the 1980s. Japan (Toshiba, NEC, and Hitachi), followed by South Korea (Samsung), China, Taiwan (notably TSMC), and select European countries (such as ASML Holding from the Netherlands), have markedly expanded their market share in recent years. Currently, the US accounts for a mere 10 percent of global commercial chip production, yet it maintains its leadership in design, research, and development.[24] Chip production involves processing such as design, manufacturing, and packaging. Integrated Device Manufacturer (IDM) companies like Intel encompass all these facets, while Fabless entities like Qualcomm focus solely on design, and Foundry firms such as TSMC specialize in manufacturing semiconductors designed by Fabless companies. The semiconductor industry comprises both memory and logic chip markets, with the latter dominating (approximately 70 percent). While South Korea leads in memory chips, necessitating economies of scale for mass production, the US concentrates on logic chips, demanding skilled architects leveraging cutting-edge technology. Geographically, chip manufacturing remains highly concentrated, posing significant supply chain risks (NIST).

The globalization wave in chip manufacturing, catalyzed by events such as China's entry into the World Trade Organization (WTO), has encountered headwinds. Trends towards nationalist economic policies post-global financial crisis and exacerbated by the COVID-19 pandemic have spurred a shift towards homeland economics. Recognizing the strategic importance of chip manufacturing, particularly in bolstering national security, initiatives like the 2021 Facilitating American-Built Semiconductors (FABS) Act and the 2022 CHIPS and Science Act have emerged. These measures encompass substantial investment tax credits and grants to stimulate domestic chip manufacturing and research while prioritizing investment in American workers (see White House briefing, August 9, 2022).

This section uses Revelio's scrape of global employment records as of March 2023 to

[24] See http://www.chips.gov.

examine the composition, skill distribution, and employment patterns of the active chip manufacturing workforce. Section C.1 describes the geographic and economic characteristics of employees with chip manufacturing skills worldwide. Section C.2 focuses on the specific chip-related skills represented in the US workforce. Section C.3 identifies the top global employers of individuals with these skills and analyzes their seniority structure. Finally, Section C.4 analyzes job outcomes for recent student cohorts who share educational backgrounds with individuals trained in chip manufacturing.

C.1 Geographic and Economic Characteristics

Table B7 provides the distribution of the physical location of 1.6 million active employees with chip manufacturing skills as of March 2023 in the world. Note that these people are not necessarily working for a chips company, nor are they necessarily working for a local company, all of which we will address later. United States is at the top of the list of countries that host these skills, with 680,602 employees physically living in the United States.[25] [26] A large fraction (480,193) of these employees work as an engineer, while 49,515 are scientists. An average employee has been at her current job, which is the 5.5^{th} one over her career, for 2,819 days (almost 8 years), with an average seniority of level 3 (associate level) out of 7.

[Table B7 about here]

India has 165,352 employees with chip skills, and a larger fraction of these people (almost 130,000) are engineers. The United Kingdom ranks third with a total of 88,527 employees, heavily skewed towards engineering roles with 57,927 engineers. Table B7 further illustrates

[25] To assess Revelio's coverage, we compared its data with the Statistics of US Businesses (SUSB) Annual Data Tables, focusing on five 6-digit NAICS codes relevant to our study: 333242, 333994, 334413, 334418, and 334515. In 2017, Revelio reported 2,070 firms in these categories, while the US Census documented 2,653. This comparison indicates that Revelio's dataset captures a substantial portion of the US chip manufacturing industry, providing a reliable representation of the sector.

[26] The strong presence of the US in the rankings likely reflects LinkedIn's user demographics, which are heavily skewed toward individuals seeking employment in the US or with US-based companies. Major competitors in the semiconductor industry, such as those in Taiwan, China, and South Korea, may not be fully represented due to LinkedIn's limited penetration in these regions. Consequently, Table 1 may not provide a fully accurate depiction of the global labor market.

that countries such as India, Brazil, Pakistan, Turkey, and Malaysia have a significant number of engineers with chip manufacturing skills and experience, as indicated by their job positions and tenure lengths. Figure B10 further illustrates the global distribution of employees with chip manufacturing skills who are actively employed as of March 2023, including countries not shown in Table B7.

[Figure B10 about here]

C.2 Chip Manufacturing Skills in the US

While Table B7 shows the United States as the leading country in terms of the number of employees skilled in chip manufacturing, it does not specify the particular skills these employees possess. Therefore, Figure B11 highlights the list of skills utilized to identify individuals with chip manufacturing expertise, alongside the percentage representation of each skill among employees in the US. The variation in skill distribution reveals both the core and peripheral abilities that contribute to the US chip manufacturing sector's operational breadth.

[Figure B11 about here]

As shown in Figure B11, skills such as *Plasma Etch* (71.99%), which is a critical skill in the fabrication of semiconductors for carving fine patterns on the surface of silicon wafers, and *Design Of Experiments* (67.67%), another important skill for estimating defect and scrap rates, which is critical to maximize profitability, exhibit substantial prevalence in the American workforce.[27] Similarly, *Chemical Vapor Deposition* (67.39%), used to create high-quality thin films, underscores its importance. Beyond these specialized skills, our data set

[27]These skills, often associated with manufacturing, are crucial in R&D and design, particularly for optimizing designs for manufacturability, minimizing defects, and ensuring seamless scalability in production. Moreover, the LinkedIn dataset likely captures roles across the semiconductor ecosystem, including US-based operations of global firms involved in advanced packaging, testing, and process development. This reflects the interconnected nature of design, R&D, and manufacturing processes in the industry

encompasses broader skill categories, including *Semiconductor Manufacturing*, where 57.58% of the global workforce is based in the US.

On the other end of the spectrum, other skills such as *Proteus* (9.98%), an important skill for reducing carbon footprint of semiconductor manufacturing, *Autosar* (11.32%), a critical skill in the design and development of automotive electronics, which are increasingly dependent on sophisticated semiconductor devices, and *Electrical Machines* (15.18%), which refers to knowledge in operating electrical machinery, reveal a lesser extent of representation.[28] Overall, Figure B11 indicates that the US holds a leading role in certain key skills within the chip manufacturing sector, yet there remains room for expanding its presence in additional skill areas.[29]

The above findings indicate that while the US has the highest number of employees with chip manufacturing skills, it does not dominate in all specific skills within the chip manufacturing sector. A considerable portion of these skills are found in the workforce outside the US. This leads to questions about the utilization of individuals who possess chip-making skills. To address this, our subsequent analysis focuses on the employment distribution of chip manufacturing talent. We begin by identifying the companies that employ these individuals and then assess their distribution across various industries, comparing those directly involved in chip manufacturing with those in unrelated sectors.

[Table B8 about here]

C.3 Top Employers of Top Chip Manufacturing Skills

Table B8 provides the list of top employers of the global workforce with chip manufacturing skills. Intel Corporation is not surprisingly the number one, and the US government, perhaps more surprisingly, is the number two on the list, with almost 30,000 and 13,400

[28] In February 2024, the Biden-Harris Administration announced a deal to allocate $1.5 billion from the CHIPS and Science Act to enhance semiconductor production related to the US auto industry. See https://bit.ly/3I3e3R1.

[29] See, e.g., more information on Plasma Etch, Design of Experiments, Chemical Vapor Deposition, and Autosar by clicking on each item.

employees, respectively.[30] Government entities such as the United States Navy, US Air Force, The United States Army, Sandia National Laboratories, Jet Propulsion Laboratory, Federal Aviation Administration, US Department of Defense, Lawrence Livermore National Laboratory, and the National Aeronautics & Space Administration are notable employers of individuals skilled in chip manufacturing. Qualcomm is in the top five of employers, with a similar number of employees (10,000–11,000) to Apple and Amazon, which seem to have hired individuals with these skills. This said, based on the composition of seniority in Table B8, Apple and Amazon hired employees with chip skills before the protectionist era and/or primarily for senior roles, rather than junior roles.

There are also non-US companies like Siemens from Germany and NPX Semiconductors from the Netherlands at the top of the list. The "Other Employers" category encompasses a significant portion of the workforce, highlighting the extensive demand and versatility of chip manufacturing skills across diverse sets of companies and sectors. In general, the table illustrates a wide-ranging employment spectrum for professionals with chip manufacturing capabilities, extending from conventional chip manufacturing firms to governmental agencies and software companies worldwide.

Table B8 also showcases the concentration of expertise and experience within these organizations. Intel Corp stands out with the majority of its 15,397 employees at Seniority Level 2, emphasizing strong mid-level expertise in its workforce. Qualcomm Inc, with 3,461 employees, sees its largest group at Seniority Level 4, suggesting a workforce with advanced experience and expertise. At the more advanced Seniority Levels 5, 6, and 7, Intel Corp leads, highlighting its leadership in highly experienced and specialized personnel.

[Table B9 about here]

Table B9 focuses on the industry composition of 680,602 active workforce with chip manufacturing in the US. Panel A identifies core chip manufacturing sectors, with "Semiconductor

[30] We conducted additional analyses to validate our employee count data, focusing on key chip manufacturers central to our study (not tabulated). For example, our records show Intel with over 119,000 employees in 2022, aligning closely with publicly reported figures of approximately 120,000 employees.

and Related Device Manufacturing" leading at 72,512 employees, followed by "Semiconductor Machinery Manufacturing" and "Instrument Manufacturing for Electricity & Electrical Signal Testing" with 7,943 and 6,514 employees, respectively. Panel B explores employment in non-chip manufacturing industries, where "Software Publishers" top the list with 35,572 professionals, and "Colleges, Universities, and Professional Schools" employ 27,661. These include academic positions, postdocs, researcher roles at universities, and related labs. Other important sectors include "Radio/TV Broadcasting & Wireless Communications Equipment Manufacturing" and "Internet Publishing and Broadcasting and Web Search Portals," housing 14,591 and 13,512 professionals, respectively.

To summarize, this section shows that the US is at the forefront in terms of active chip manufacturing workforce, housing approximately 600,000 of the global 1.6 million experts in this field. However, it appears that the US does not fully capitalize on its chip manufacturing workforce's potential because many individuals with chip manufacturing skills work at jobs outside the chip manufacturing industry.

C.4 Yearly Cohorts of Students Proficient in Chip Manufacturing Skills

Using our unique data covering the educational characteristics of various cohorts of students around the world, we also present summary statistics on related education and job outcomes. Panel A of Figure B1 offers a look into the first career steps taken by US graduates who shared the same graduation year, program, and university with individuals possessing chip manufacturing skills. This analysis is segmented by degree type and initial job category chosen post-graduation. For job category classification, we employ Revelio's clustering algorithms, which sort jobs into seven primary categories: Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist. The data is as of the end of 2017, and the figure excludes counts of classmates below 1,000 to enhance readability.

[Figure B1 about here]

The cohort size for 2017 totals 109,126. Bachelor's degree holders (65,290) predominantly pursued engineering, with 42,100 graduates, followed by roles in science (6,184) and sales (5,862). For those with doctoral degrees, there is a pronounced preference for scientific (2,180) and engineering (1,282) positions, underscoring a career focus on research and technical development within the chip manufacturing field. Master's degree recipients show a preference for engineering (25,693) and science (3,600), with additional graduates moving into administrative, financial, marketing, operational, and sales positions. MBA graduates show a diverse range of initial job preferences, with significant numbers entering engineering (1,136) and sales (1,043), along with finance (801) and operations (543).

Overall, Panel A of Figure B1 illustrates that prior to US protectionist policies, individuals with a Bachelor's degree exhibited a preference for roles within the technical and commercial sectors. Those with doctorate and master's degrees predominantly pursued careers in science and engineering. On the other hand, there is a tendency among MBA graduates to seek positions that combine technical expertise with strategic and commercial insight.

D Additional Findings

D.1 Additional Summary Statistics

We start with presenting summary statistics for cohorts in Panel A of Table B10, using 35,496 observations between 2014 and 2022 at the country-degree-job category-year level that capture the size of each cohort that take job type j after graduating from the same degree d from the same university in country c in year t, along with their average salary, seniority, and tenure in their first jobs, respectively. As shown, the average logged classmate size choosing job type j –Log(Cohort Size$_{c,d,j,t}$)– is equal to 1.21. While the average logged salary is equal to 6.02, the average seniority stands at 1.51, with a close median of 1.50, reflecting a relatively uniform early career progression among these individuals. Meanwhile, the tenure of these positions, Log(Tenure$_{c,d,j,t}$), has a mean (median) of 3.18 (5.02).

D.2 Using Non-US Engineers and Scientists as Control Units

A potential concern with our main analysis is that our choice of comparison group—specifically, jobs in finance, marketing, sales, operations, and administration—may not provide the most appropriate counterfactual for science and engineering roles. If semiconductor firm employment expanded overall during this period, as suggested by broader hiring patterns, then science and engineering jobs could have remained stable or even grown in absolute terms while declining only in relative terms compared to other functions. This would make the economic interpretation of our findings less clear, as relative declines might reflect business strategy shifts rather than policy-induced constraints. Moreover, it remains unclear whether science and engineering positions were the primary intended targets of protectionist policies, given that political rhetoric largely emphasized protecting blue-collar manufacturing workers rather than high-skilled technical roles. An alternative interpretation of our results is that firms strategically expanded non-technical functions—perhaps in response to increased regulatory compliance, supply chain complexity, or domestic market focus—while maintaining

stable technical workforces. Such a pattern would not necessarily indicate policy failure if the goal was broad-based employment growth.

To address these concerns, Table B1 presents results using a more restrictive identification strategy that compares "apples with apples." We focus exclusively on scientists and engineers, contrasting employment patterns between US and non-US operations within the same firm and year. This approach isolates the geographic effects of US protectionist policies while holding constant firm-specific factors, technological requirements, and skill demands. Panel A shows that US-based scientists and engineers experienced significant declines in employment (8%), hiring (16%), separations (12%), and turnover (19%) compared to their non-US counterparts at the same firms. Panel B confirms these patterns across different career progression stages, with particularly pronounced effects on first-job scientists and engineers (5% decline) and experienced hires (8% decline). The consistency of these within-firm, cross-geography comparisons strengthens confidence that our main findings reflect genuine policy impacts on technical employment rather than compositional changes in firm hiring strategies.

D.3 Disentangling Industry-Specific Effects from Broader Tech Trends

In this section, we investigate whether our baseline results hold after excluding roles related to data science and programming. Remember that our primary analyses compare engineers and scientists to non-technical staff within each US chip manufacturing firm in a given year, examining changes before and after the onset of protectionist policies in the US. The engineer and scientist positions include a broad spectrum of technical roles, including various engineering disciplines (e.g. manufacturing, automation, system test, mechanical), as well as technician roles (e.g., assembly, quality inspection, technical support) and R&D positions.

Within the engineer and scientist category, we recognize the presence of data science and software roles.[31] Although these positions constitute a small portion of the chip manufacturing workforce, their increasing prominence, coinciding with US protectionist policies,

[31] For example, we estimate a reduction of -5.58% in IT Project Manager roles in Appendix Figure B4.

warrants careful analysis. For instance, the decline in the number of scientists and engineers may be partially attributed to individuals transitioning from the chip manufacturing sector to roles in data science or technology companies. To ensure the robustness of our findings, we conduct a targeted analysis of job titles, systematically identifying and excluding data science and programming roles.[32] This strategic exclusion serves a dual purpose: it allows us to isolate the true impact of protectionist policies on core chip manufacturing roles, and it eliminates potential confounding effects from broader tech industry trends.

By focusing on employees most likely to transition to data science and programming roles in other sectors, we effectively control for cross-industry labor flows. This refined approach strengthens our analysis, providing a more precise measure of the impact of protectionist policies on the chip manufacturing workforce. We then reestimate our regressions using this adjusted dataset, reinforcing the validity and specificity of our results.

As shown in Panel A of Table B11, the estimated effects on the log number of scientists and engineers, as well as on hiring, separation and turnover, remain economically and statistically significant. Panels B and C of Table B11 further report estimates on employment growth rates and the heterogeneity of effects by career progression. These collective results reinforce the robustness of our findings presented in Section 4.1. They demonstrate that our main findings persist even when accounting for potential career transitions of data scientists and software engineers – the groups most prone to migrating to similar roles outside of the chip manufacturing industry. This consistency highlights the specific impact of protectionist policies on the semiconductor workforce, distinct from broader tech sector trends.

The consistency of effects across diverse specifications of this robustness section strengthens confidence that our findings reflect genuine causal impacts of protectionist policies rather

[32] In particular, we search for job titles containing terms such as "data," "software," and "programming," which leads us to the following job titles: "advisory software engineer," "analyst programmer," "business data analyst," "clinical data," "computer programmer," "data analyst," "data architect," "data center," "data engineer," "data science," "data scientist," "database administrator," "database developer," "embedded software engineer," "java software developer," "oracle database administrator," "software architect," "software developer," "software engineer," "software quality assurance engineer," and "systems programmer."

than spurious correlations or methodological artifacts.

D.4 Additional Tests on Annual Cohorts of Chip Manufacturing Education Using Data From The Department of Education

In the main text, we utilize Revelio data to examine cohorts of students who enter chip manufacturing careers along with their classmates. In this section, we revisit this question using data from the US Department of Education on degree completions in the US In particular, we use the Integrated Postsecondary Education Data System (IPEDS), which is part of the National Center for Education Statistics (NCES). This data is not self-reported and, therefore, less prone to measurement issues, and it allows us to double-check our earlier findings with a second dataset.

NCES data is publicly available at https://nces.ed.gov/ipeds/datacenter/ under 'Complete Data Files' and 'Completions'. These files contain detailed information on the number of graduates from each institution in the US (identified with unique UNITID identifiers) across different degrees (denoted with unique 6-digit CIPCODE identifiers) and degree levels (AWLEVEL). The number of graduates is measured in aggregate (CTOTALT) and based on visa status (CNRALT), which measures the number of Non-US graduates, referring to students who are not citizens or nationals of the United States, i.e., in the country on a visa or temporary basis without the right to remain indefinitely.

We focus on students' initial major completions and identify degree programs (CIP codes) related to chip manufacturing by analyzing the NCES CIP code descriptions, which explain how each degree prepares students for specific careers.[33] These files define each degree type in the US (consistently across institutions) and describe the career preparation each degree offers. For example, CIP code '15.0616' refers to '*Semiconductor Manufacturing Technology/Technician*' and is described as a 'program that prepares individuals to apply basic engineering principles and technical skills to operate and monitor equipment for the fabrica-

[33]These descriptions are publicly available here: https://nces.ed.gov/ipeds/cipcode/resources.aspx?y=56. See, e.g., the CIP Codes 2020 spreadsheet.

tion of semiconductors or microchips from silicon wafers, and to troubleshoot, maintain, and repair the specialized equipment used in this process. Includes instruction in AC and DC circuits, digital fundamentals, solid state devices, manufacturing processes, vacuum principles and technology, industrial electronics, quality assurance, and semiconductor manufacturing technology.'

Using NCES degree descriptions, we identify US engineering and technician degrees where the CIP family (the first two digits of the CIP code) is 14, 15, 46, 47, or 48. We then determine which of these degrees are related to chip manufacturing by searching program titles, CIP definitions, and examples for keywords `chip|semicond|circuit|wafer|silicon|microelec|fabless|microchip|MEMS|lithograph|etching|microfab|photonic|manufact` in regular expressions.

In doing so, we identify the following chip manufacturing-related engineering and technician degrees (with their corresponding CIP codes).[34] We categorize these degrees in Bachelor & Pre-Bachelor categories (i.e., 1<AWLEVEL<=5) and Graduate categories (i.e., AWLEVEL==7 or AWLEVEL==7):

- 140103: Applied Engineering
- 140902: Computer Hardware Engineering
- 141801: Materials Engineering
- 141901: Mechanical Engineering
- 143601: Manufacturing Engineering
- 144701: Electrical and Computer Engineering
- 150001: Applied Engineering Technologies/Technicians
- 150303: Electrical, Electronic, and Communications Engineering Technology/Technician
- 150306: Integrated Circuit Design Technology/Technician
- 150403: Electromechanical/Electromechanical Engineering Technology/Technician
- 150613: Manufacturing Engineering Technology/Technician

[34]The following CIP codes and titles were identified as false positives and excluded from the treatment group: 141004 (Telecommunications Engineering), 142001 (Metallurgical Engineering), 142801 (Textile Sciences and Engineering), 144001 (Paper Science and Engineering), 144101 (Electromechanical Engineering), 144501 (Biological/Biosystems Engineering), 144802 (Power Plant Engineering), 150607 (Plastics and Polymer Engineering Technology/Technician), 150611 (Metallurgical Technology/Technician), 150801 (Aeronautical/Aerospace Engineering Technology/Technician), 150803 (Automotive Engineering Technology/Technician), and 150806 (Marine Engineering Technology/Technician).

- 150616: Semiconductor Manufacturing Technology/Technician
- 150617: Composite Materials Technology/Technician
- 150702: Quality Control Technology/Technician
- 150805: Mechanical/Mechanical Engineering Technology/Technician
- 151201: Computer Engineering Technology/Technician
- 151203: Computer Hardware Technology/Technician
- 151305: Electrical/Electronics Drafting and Electrical/Electronics CAD/CADD
- 151306: Mechanical Drafting and Mechanical Drafting CAD/CADD
- 151307: 3-D Modeling and Design Technology/Technician
- 151501: Engineering/Industrial Management
- 470101: Electrical/Electronics Equipment Installation and Repair Technology/Technician, General
- 470105: Industrial Electronics Technology/Technician
- 470302: Heavy Equipment Maintenance Technology/Technician
- 480501: Machine Tool Technology/Machinist
- 480503: Machine Shop Technology/Assistant
- 480511: Metal Fabricator

The strategy above provides a sample of students that closely matches our Revelio data in terms of relevant programs and student numbers. For instance, Revelio data includes an undergraduate cohort of 65,290 students in chip manufacturing-related education, while IPEDS data, as of 2017, lists 60,990 students in similar programs. We classify chip manufacturing-related degrees as treated units and all other degrees as control units, comparing both groups before and after the onset of the protectionist era in 2018. We employ the below difference-in-differences specification:

$$y_{d,t} = \tau \text{Treated}_d \times \text{Post}_t + \gamma_d + \theta_t + \epsilon_{d,t}. \tag{D.21}$$

Our analysis focuses on $y_{d,t}$, which represents either Log(Completions$_{d,t}$), Log(US Resident Completions$_{d,t}$), or Log(Non-US Resident Completions$_{d,t}$). These denote, respectively, the number of all students graduating from degree d in the US in year t, the number of US

resident students graduating from degree d in the US in year t, and the number of non-US resident students graduating from degree d in the US in year t. Treated_d is set to one for the chip manufacturing-related engineering and technician degrees mentioned above, and zero otherwise. Post_t is one for years after 2018 and zero otherwise. Table B3 presents our findings.

[Table B3 about here]

As shown in Table B3, we identify a 14% decline in the number of graduates from bachelor and pre-bachelor degrees in the US (Panel A, Column 1) and a 14% decline in postgraduate degrees (Panel B, Column 1). Furthermore, the reduction in the number of non-US resident graduates is also significant, amounting to nearly 17% and 29% in undergraduate and postgraduate programs, as shown in Columns 2 and 4, respectively. There is a decline in degree completions among US residents at the bachelor's and pre-bachelor levels, while graduate-level completions have slightly increased. These can be seen in column 2 of panels A and B. Overall, these results align with our findings based on the Revelio data shown in Panel A of Table 5, collectively suggesting a reduction in the number of chip manufacturing students in the post-protectionist era.

D.5 Other Findings

In this section, we present supplementary results not included but mentioned in the main text or earlier parts of this section. Appendix Table B12 shows the results of our placebo test, examining the impact of US protectionist policies on employment in science and engineering roles within US firms, specifically those classified under the NAICS code 423690. This sector includes businesses primarily focused on the merchant wholesale distribution of electronic parts and equipment. Examples of firms in this category include wholesalers of blank CDs/DVDs (as opposed to manufacturers of wafers) and blank diskettes (as opposed to manufacturers of chips). Our findings indicate no significant effects of US protectionism

on the employment levels within these firms. Appendix Figures B2, B3, and B6 present effect dynamics and evidence for the observable counterpart of the parallel trends assumption for all other dependent variables from Tables 2 and 5 that were not displayed in the main body of the text.

Appendix Table B1. **Main Results Using Non-US Engineers and Scientists as Control Units**

This table presents our findings on the effects of protectionism on science and engineering employment by comparing the number and composition of scientists and engineers employed at US chip manufacturers across their US and non-US operations, within the same company-year. We present estimates based on the following specification:

$$y_{i,c,t} = \beta \text{US}_c \times \text{Post}_t + \alpha_{i,t} + \gamma_{i,c} + \varepsilon_{i,c,t}.$$

Our dependent variables are defined as follows. *Log(SciEngEmp$_{i,c,t}$)*, is the log of one plus the number of scientists and engineers employed at company i in country c in year t. *Log(SciEngHire$_{i,c,t}$)* is the log of one plus the number of new scientist and engineer hires at company i in country c in year t. New hires are defined as scientists and engineers whose first year at the firm is t. *Log(SciEngSep$_{i,c,t}$)* is the log of one plus the number of scientists and engineers who left company i in country c in year t. This refers to employees, whose final year of employment at firm i is t. *Log(SciEngTurn$_{i,c,t}$)* is the log of one plus the total number of scientist and engineer hires and separations at company i in country c in year t. *Log(FirstJobSciEng$_{i,c,t}$)* is the log of one plus the number of newly hired scientists and engineers at company i in country c in year t who are entering their first job and have no prior work experience. *Log(ExprSciEng$_{i,c,t}$)* is the log of one plus the number of newly hired scientists and engineers with prior work experience. *Log(JunPosSciEng$_{i,c,t}$)* is the log of one plus the number of newly hired scientists and engineers in junior positions (Revelio seniority levels 1–3). *Log(MidSenSciEng$_{i,c,t}$)* is the log of one plus the number of newly hired scientists and engineers in mid-senior positions (Revelio seniority levels 4–5). *US$_c$* equals one if country c is the US, and zero otherwise. *Post$_t$* takes a value of one for the years after 2018 and zero for the preceding years. $\alpha_{i,t}$ and $\gamma_{i,c}$ refer to firm-year and firm-country fixed effects, respectively. Section B of the Appendix offers detailed information on the data collection process. The analysis covers 2014–2022, with standard errors clustered by firm. Significance at the 1%, 5%, and 10% levels is indicated by ***, **, and *, respectively.

Panel A: Comparing Scientists/Engineers in US vs. Abroad within the Same Firm-Year (N=63,378)				
	Log(SciEngEmp$_{i,c,t}$)	Log(SciEngHire$_{i,c,t}$)	Log(SciEngSep$_{i,c,t}$)	Log(SciEngTurn$_{i,c,t}$)
	(1)	(2)	(3)	(4)
US$_c$ × Post$_t$	-0.08***	-0.16***	-0.12***	-0.19***
	(-5.34)	(-10.36)	(-6.70)	(-9.34)
Firm × Year FE	Yes	Yes	Yes	Yes
Firm × Country FE	Yes	Yes	Yes	Yes
Panel B: Comparing Scientists/Engineers in US vs. Abroad by Career Progression (N=63,378)				
	Log(FirstJobSciEng$_{i,c,t}$)	Log(ExprSciEng$_{i,c,t}$)	Log(JunPosSciEng$_{i,c,t}$)	Log(MidSenSciEng$_{i,c,t}$)
	(1)	(2)	(3)	(4)
US$_c$ × Post$_t$	-0.05***	-0.08***	-0.07***	-0.03***
	(-5.75)	(-5.17)	(-4.49)	(-3.20)
Firm × Year FE	Yes	Yes	Yes	Yes
Firm × Country FE	Yes	Yes	Yes	Yes

Appendix Table B2. **US Job Postings for Scientists and Engineers**

This table presents our findings on the influence of protectionism on job postings in the US. We present estimates based on the following specification:

$$y_{j,t} = \alpha + \beta \text{Treated}_j \times \text{Post}_t + \gamma_j + \delta_t + \varepsilon_{j,t},$$

where j indexes job categories and t indexes years. Our dependent variables are defined as follows. *Log(JobPostCreation$_{j,t}$)* is the log of one plus the number of new job posts in category j in year t. *Log(JobPostDeletion$_{j,t}$)* is the log of one plus the number of deleted job posts in category j in year t. *Log(ActiveJobPosts$_{j,t}$)* is the log of one plus the number of active job postings in category j as of year t. The job posting data is sourced from LinkUp. In Panel A, *Treated$_j$* equals one for job categories classified as scientist or engineer roles and zero for all other categories. We exclude "Medical Representative" and "Geologist" from the treated categories to focus specifically on engineers and scientists. In Panel B, we further refine *Treated$_j$* by excluding "Data Analyst," "IT Project Manager," "IT Specialist," "Software Engineer," and "Sustainability Specialist." The final treated job categories include "Engineer," "Production Operator," "QA Tester," "Quality Assurance," "Scientist," "Technical Architect," and "Technician." *Post$_t$* takes a value of one for the years after 2018 and zero for the preceding years. The analysis spans from 2014 to 2022, with standard errors clustered by job category. Section B of the Appendix offers detailed information on the data collection process. Significance levels of 1%, 5%, and 10% are denoted by $\star\star\star$, $\star\star$, and $\star$, respectively.

Panel A: Job Posts for Engineers and Scientists			
	Log(JobPostCreation$_{j,t}$)	Log(JobPostDeletion$_{j,t}$)	Log(ActiveJobPosts$_{j,t}$)
	(1)	(2)	(3)
Treated$_j$ × Post$_t$	0.11**	0.11**	0.13***
	(2.40)	(2.49)	(2.82)
Job Category FE	Yes	Yes	Yes
Year FE	Yes	Yes	Yes
Observations	432	432	432
R-squared	0.981	0.981	0.983
Panel B: Findings After Excluding Job Posts for Software Engineers, IT, and Data Science			
	Log(JobPostCreation$_{j,t}$)	Log(JobPostDeletion$_{j,t}$)	Log(ActiveJobPosts$_{j,t}$)
	(1)	(2)	(3)
Treated$_j$ × Post$_t$	0.12**	0.12***	0.13***
	(2.69)	(2.70)	(3.18)
Job Category FE	Yes	Yes	Yes
Year FE	Yes	Yes	Yes
Observations	387	387	387
R-squared	0.981	0.981	0.983

Appendix Table B3. **Protectionism and US Chip Manufacturing Degree Completions: Evidence from IPEDS Data by Residency Status**

This table reports the estimated effects of protectionism on chip manufacturing degrees obtained in the US. We present estimates based on the following specification:

$$y_{d,t} = \alpha + \beta \text{Treated}_d \times \text{Post}_t + \gamma_d + \delta_t + \varepsilon_{d,t},$$

where d indexes degree categories and t indexes years. The data is sourced from the US Department of Education's Integrated Postsecondary Education Data System (IPEDS), focusing on degree completions in the US for all students, US residents and non-US residents. *Treated*$_d$ equals one for degree categories including US engineering and technician degrees where the CIP family (the first two digits of the CIP code) is 14, 15, 46, 47, or 48. We determine which of these degrees relate to chip manufacturing by searching program titles, CIP definitions, and descriptions for keywords `chip|semicond|circuit|wafer|silicon|microelec|fabless|microchip|MEMS|lithograph|etching|microfab|photonic|manufact` using regular expressions. Control degrees include all other degrees. *Log(Total Completions*$_{d,t}$*)*, *Log(US Resident Completions*$_{d,t}$*)*, and *Log(Non-US Resident Completions*$_{d,t}$*)* represent the number of all students graduating from degree d in the US in year t, the number of US resident students graduating from degree d in the US in year t, and the number of non-US resident students graduating from degree d in the US in year t, respectively. *Treated*$_d$ is set to one for the chip manufacturing-related engineering and technician degrees mentioned above and zero otherwise. *Post*$_t$ is one for years after 2018 and zero otherwise. γ_d and δ_t refer to degree and year fixed effects. Clustering is done at the CIP degree family level. See Section D.4 for additional variable descriptions and methodology. For detailed information on data collection methods and detailed definitions of the variables, please see Section D.4. Statistical significance at the 1%, 5%, and 10% levels are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Bachelor & Pre-Bachelor Degrees			
	Log(Total Completions$_{d,t}$)	Log(US Resident Completions$_{d,t}$)	Log(Non-US Resident Completions$_{d,t}$)
	(1)	(2)	(3)
Treated$_d$ × Post$_t$	-0.14***	-0.14***	-0.17***
	(-3.87)	(-3.53)	(-4.83)
Degree FE	Yes	Yes	Yes
Year FE	Yes	Yes	Yes
Observations	10,980	10,980	10,980
R-squared	0.974	0.974	0.944
Panel B: Graduate Degrees			
	Log(Total Completions$_{d,t}$)	Log(US Resident Completions$_{d,t}$)	Log(Non-US Resident Completions$_{d,t}$)
	(1)	(2)	(3)
Treated$_d$ × Post$_t$	-0.14***	0.05*	-0.29***
	(-3.46)	(1.82)	(-4.19)
Degree FE	Yes	Yes	Yes
Year FE	Yes	Yes	Yes
Observations	9,044	9,044	9,044
R-squared	0.965	0.965	0.940

Appendix Table B4. **Robustness to Excluding Large Firms and Using Poisson Pseudo-maximum-likelihood (PPML) Regressions**

This table reports the estimated effects of protectionism on science and engineering employment in US chip manufacturing firms, based on the difference-in-differences approach outlined in Equation (8). We exclude the top 10% of firms by 2014 total workforce size. Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data-collection process. $Treated_j$ equals one for science and engineering job categories and zero for finance, marketing, sales, operations, and administrative categories. $Post_t$ equals one for the years after 2018 and zero for earlier years. Panel A presents results for the chip manufacturing workforce using OLS regressions in Panel A.1. Panels A.2 and A.3 report Poisson pseudo-maximum-likelihood (PPML) estimates (Correia et al. (2020)) with probability weights (inverse of firm age in 2014) and without weights, respectively. Panel B shows results by career-progression category using OLS regressions in Panel B.1. Panels B.2 and B.3 provide the corresponding PPML estimates, with and without weights. All regressions include firm-by-job-category and firm-by-year fixed effects. Each panel contains 62,082 observations covering 2014–2022. Standard errors are clustered by firm. Significance at the 1 %, 5 %, and 10 % levels is denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce (N=62,082)				
Panel A.1: Findings Based on OLS Regressions				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.04***	-0.10***	-0.05***	-0.10***
	(-3.78)	(-9.52)	(-5.02)	(-8.72)
Panel A.2: Findings Based on Poisson Pseudo-Maximum-Likelihood (PPML) Regressions				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.05***	-0.08***	-0.07**	-0.07***
	(-4.35)	(-2.89)	(-2.28)	(-3.05)
Panel A.3: Findings Based on Unweighted Poisson Pseudo-Maximum-Likelihood (PPML) Regressions				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.05**	-0.03	-0.03**
	(-4.83)	(-2.40)	(-1.52)	(-2.04)
Panel B: Science and Engineering Employment by Career Progression (N=62,082)				
Panel B.1: Findings Based on OLS Regressions				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.02**	-0.02**	-0.01
	(-3.81)	(-2.28)	(-2.26)	(-1.60)
Panel B.2: Findings Based on Poisson Pseudo-Maximum-Likelihood (PPML) Regressions				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.05***	-0.05***	-0.06***	-0.06***
	(-3.28)	(-3.66)	(-3.87)	(-3.45)
Panel B.3: Findings Based on Unweighted Poisson Pseudo-Maximum-Likelihood (PPML) Regressions				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.04***	-0.03***	-0.04***	-0.03**
	(-4.26)	(-3.18)	(-4.98)	(-2.34)

Appendix Table B5. **Findings on Patenting Activities Based on Poisson Pseudo-Maximum-Likelihood (PPML) Regressions**

This table presents our findings on how US protectionism has influenced patenting activities of chip manufacturing firms. Our estimates are derived from a Poisson pseudo-likelihood regression with multiple levels of fixed effects (Correia et al., 2020). Panels A and B report our estimates with probability weights (inverse of firm age in 2014) and without weights, respectively. The sample is a firm–year panel (2014–2022) based on Revelio's "Assignee Matches" dataset. We retain firms that filed at least one patent during our sampling period. *Log(Patents Filed$_{i,t}$)* and *Log(Patents Granted$_{i,t+2}$)*, are the natural logs of one plus the number of patents firm i files in year t and is granted in year t+2, respectively. *US Firm$_i$* is equal to one if firm i is a US firm based on PatentsView classification. *Post$_t$* takes a value of one for the years after 2018 and zero for the preceding years. *Sponsor$_i$* indicates whether firm i sponsored an H-1B petition in fiscal year 2017 based on the USCIS H-1B Employer Data Hub. All specifications include firm fixed effects and industry(6-digit NAICS)-by-year fixed effects. Section B of the Appendix offers detailed information on the data collection process. Standard errors are clustered at the firm level, with $***$, $**$, and $*$ denoting significance at the 1%, 5%, and 10% levels, respectively.

Panel A: Findings Based on PPML Regressions (N=18,693)						
	Log(Patents Filed$_{i,t}$)			Log(Patents Granted$_{i,t+2}$)		
	(1)	(2)	(3)	(4)	(5)	(6)
US Firm$_i$ × Post$_t$	-0.27***		-0.27***	-0.30***		-0.28***
	(-3.48)		(-3.20)	(-3.88)		(-3.20)
Sponsor$_i$ × Post$_t$		-0.10	0.21		-0.16	0.06
		(-0.94)	(0.98)		(-1.58)	(0.36)
Sponsor$_i$ × US Firm$_i$ × Post$_t$			-0.21			-0.11
			(-0.88)			(-0.55)
Firm FE	Yes	Yes	Yes	Yes	Yes	Yes
Industry x Year FE	Yes	Yes	Yes	Yes	Yes	Yes
Panel B: Findings Based on Unweighted PPML Regressions (N=18,693)						
	Log(Patents Filed$_{i,t}$)			Log(Patents Granted$_{i,t+2}$)		
	(1)	(2)	(3)	(4)	(5)	(6)
US Firm$_i$ × Post$_t$	-0.13***		-0.16***	-0.22***		-0.24***
	(-3.02)		(-3.26)	(-5.18)		(-5.04)
Sponsor$_i$ × Post$_t$		0.04	0.24		-0.03	0.05
		(0.79)	(1.59)		(-0.65)	(0.49)
Sponsor$_i$ × US Firm$_i$ × Post$_t$			-0.15			0.01
			(-0.94)			(0.07)
Firm FE	Yes	Yes	Yes	Yes	Yes	Yes
Industry x Year FE	Yes	Yes	Yes	Yes	Yes	Yes

Appendix Table B6. **Findings on Cross-Country Composition of Chip Manufacturing Skills Based on Poisson Pseudo-Maximum-Likelihood (PPML) Regressions**

This table presents our findings on how US protectionism has influenced the geography of chip manufacturing skills. We present estimates based on the difference-in-differences methodology outlined in section 7.2. Our estimates are derived from a Poisson pseudo-likelihood regression with probability weights (inverse of firm age in 2014) (Correia et al., 2020). The sample is a country–year–skill panel drawn from Revelio's dynamic skills dataset, covering 245 countries and 75 skill categories. The analysis spans the years 2019–2022, the only period for which Revelio's dynamic skill data is available. The dependent variable, *Log(Skill Stock$_{s,c,t}$)*, is the logarithm of the number of LinkedIn users in country c who list or are endorsed with skill s in year t, winsorized at the 1% tails. *Chip Skill$_s$* equals one when the skill s belongs to the "electronics / semiconductors / design of experiments" category and zero otherwise. *US$_c$* equals one if country c is the US, and zero otherwise. *Post$_t$* equals one for 2020–2022 and zero for 2019. Indicator variables $\mathbf{1}[Year = t]$ take the value one in year t and zero in all other years. Section B of the Appendix offers detailed information on the data collection process. Standard errors are clustered at the skill category level. Statistical significance at the 1%, 5%, and 10% levels is denoted by $***$, $**$, and $*$, respectively.

	Log(Skill Stock$_{s,c,t}$)	Log(Skill Stock$_{s,c,t}$)	Log(Skill Stock$_{s,c,t}$)	Log(Skill Stock$_{s,c,t}$)
	(1)	(2)	(3)	(4)
Chip Skill$_s$ × US$_c$ × Post$_t$	-0.04***	-0.04***		
	(-19.95)	(-14.95)		
Chip Skill$_s$ × Post$_t$	0.04***			
	(12.00)			
Chip Skill$_s$ × US$_c$ × **1**[Year=2020]			-0.03***	-0.03***
			(-21.97)	(-17.73)
Chip Skill$_s$ × US$_c$ × **1**[Year=2021]			-0.04***	-0.04***
			(-19.72)	(-14.80)
Chip Skill$_s$ × US$_c$ × **1**[Year=2022]			-0.05***	-0.05***
			(-17.21)	(-12.63)
Chip Skill$_s$ × **1**[Year=2020]			0.03***	
			(14.31)	
Chip Skill$_s$ × **1**[Year=2021]			0.04***	
			(11.15)	
Chip Skill$_s$ × **1**[Year=2022]			0.04***	
			(10.69)	
Country FE x Skill Category FE	Yes	Yes	Yes	Yes
Country FE x Year FE	Yes	Yes	Yes	Yes
Skill Category FE x Year FE	No	Yes	No	Yes
Observations	70,247	70,247	70,247	70,247

Appendix Table B7. **Active Chip Manufacturing Workforce**

This table shows the global distribution of employees, who possess skills in chip manufacturing and are actively employed as of March 2023. Panel A aggregates the total count of these employees across locations of employees and distributes them into various job categories (Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist), as defined by Revelio's clustering algorithms. *Total Emp.* refers to the total number employees with chip manufacturing skills. Panel B outlines employment characteristics for each country: *Tenure* is the average number of days active employees with chip manufacturing skills have spent in their current position; *RN* represents the average order of a job within an employee's career; *Salary* is the average annual income in USD; and *Seniority* refers to the average seniority level, categorized into seven levels. For more details on the data collection methodology and the definition of chip manufacturing skills, refer to Section B.1.2. For detailed variable definitions, please see Section B.2.

		Panel A: Employee Count by Job Category								Panel B: Economic Characteristics			
Rank	Country	Total Emp.	Admin	Engineer	Finance	Marketing	Operations	Sales	Scientist	Tenure	RN	Salary	Seniority
1	United States	680,602	26,373	480,193	8,531	11,578	31,790	72,622	49,515	2,819.03	5.47	100,384.72	2.95
2	India	165,352	9,880	122,978	2,476	2,728	7,216	11,946	8,128	1,986.43	4.11	12,750.81	2.79
3	United Kingdom	88,527	3,728	57,927	1,033	2,121	5,687	10,888	7,143	2,543.08	5.7	58,110.89	3.02
4	Canada	63,376	2,784	44,752	758	1,223	2,770	6,229	4,860	2,407.60	5.58	61,114.26	2.70
5	Germany	43,597	1,272	28,759	261	682	1,725	4,665	6,233	2,037.52	5.7	79,377.39	2.97
6	France	38,024	1,476	25,422	349	916	1,572	3,600	4,689	2,089.61	6.08	52,630.56	2.92
7	Italy	30,545	1,236	20,301	237	697	1,557	3,660	2,857	2,832.06	5.15	55,721.32	2.81
8	Australia	30,199	1,456	20,703	407	603	1,523	3,264	2,243	2,286.17	5.88	80,238.36	2.79
9	China	28,664	1,930	16,330	306	586	1,817	5,320	2,375	3,330.75	3.66	28,236.07	3.19
10	Netherlands	28,320	1,180	18,415	225	755	1,501	2,913	3,331	2,513.68	6.31	64,067.80	2.89
11	Brazil	25,968	1,999	17,787	466	497	1,415	2,396	1,408	2,711.02	5.48	14,588.81	2.51
12	Israel	21,956	572	16,511	103	275	889	1,516	2,090	2,395.99	4.99	73,976.56	3.16
13	Spain	20,989	1,166	14,450	176	493	724	1,708	2,272	2,413.65	5.62	50,341.81	2.72
14	Singapore	18,648	607	12,547	291	244	1,238	2,215	1,506	2,395.93	4.86	46,346.70	3.2
15	Pakistan	18,232	1,820	12,539	198	380	925	1,290	1,080	2,453.57	4.13	13,330.76	2.64
16	Mexico	18,137	843	13,291	175	260	1,237	1,464	867	2,643.00	5.01	29,523.58	2.79
17	Sweden	17,869	561	12,241	83	269	837	1,691	2,187	2,164.33	6.55	66,023.95	2.91
18	Turkey	16,575	885	11,537	125	290	589	1,626	1,523	2,034.55	5.02	20,327.08	2.69
19	Taiwan	16,312	565	10,919	142	221	960	2,320	1,185	3,233.21	3.86	76,870.21	3.25
20	Malaysia	13,874	706	10,613	168	141	730	948	568	2,654.82	4.13	21,392.26	2.85
	Other Countries	285,143	16,541	195,247	2,763	5,505	13,647	26,783	24,657	2,524.85	5.07	48,186.61	2.78

Appendix Table B8. **Top 25 Employers of Active Chip Manufacturing Workforce**

This table ranks the top 25 firms by the number of active employees around the globe with chip manufacturing skills as of March 2023. *Total Emp.* refers to the total number employees with chip manufacturing skills. *Seniority* is classified into seven levels, reflecting the hierarchical position within the company. In the case of multiple employers for a given employee, we keep the employer matching with the employee's highest job seniority. Further information on how data was gathered and the specific criteria used to identify chip manufacturing skills can be found in Section B.1.2. For detailed variable definitions, please see Section B.2.

			Seniority						
Rank	Employer	Total Emp.	1	2	3	4	5	6	7
1	Intel Corp.	29,178	1,268	15,397	3,658	3,787	4,344	697	27
2	Government of the USA	13,361	4,893	5,590	891	1,001	914	41	31
3	Apple, Inc.	11,956	449	7,589	1,259	1,177	1,382	96	4
4	Amazon.com, Inc.	10,976	327	4,115	1,677	2,325	2,188	338	6
5	QUALCOMM, Inc.	10,427	78	2,233	2,330	3,461	1,783	539	3
6	Siemens AG	9,063	540	3,977	1,618	1,551	1,203	153	21
7	Alphabet, Inc.	7,877	119	5,561	716	701	686	91	3
8	Raytheon Technologies Corp.	7,455	674	2,784	1,000	1,390	1,497	108	2
9	Advanced Micro Devices, Inc.	7,148	79	2,420	1,234	1,887	1,130	392	6
10	Microsoft Corp.	6,849	150	4,274	582	640	948	243	12
11	NXP Semiconductors NV	6,546	296	2,319	1,068	1,246	1,362	248	7
12	Robert Bosch Stiftung GmbH	6,457	523	3,819	740	658	587	124	6
13	Infineon Technologies AG	6,196	373	2,534	817	891	1,377	183	21
14	Texas Instruments Inc.	6,059	279	2,372	698	1,186	1,293	225	6
15	Samsung Electronics Co., Ltd.	5,996	395	2,615	580	666	1,520	213	7
16	Schneider Electric SE	5,560	572	2,532	727	810	771	138	10
17	Honeywell International, Inc.	5,434	593	3,064	489	609	586	85	8
18	STMicroelectronics NV	5,363	257	2,283	966	1,090	678	85	4
19	IBM Corp.	5,220	126	1,748	798	1,429	978	118	23
20	Analog Devices, Inc.	5,083	351	2,139	743	902	802	142	4
21	Broadcom, Inc.	5,076	159	1,537	647	802	1,799	127	5
22	NVIDIA Corp.	5,057	41	2,188	927	747	946	206	2
23	ABB Ltd.	4,960	378	2,313	693	809	703	57	7
24	Micron Technology, Inc.	4,883	236	1,260	595	1,056	1,427	302	7
25	Applied Materials, Inc.	4,693	163	1,343	680	936	1,236	316	19
	Other Employers	1,371,038	189,604	538,598	158,650	200,048	215,743	39,044	29,351

Appendix Table B9. **Industry Composition of Active Chip Manufacturing Workforce**

This table displays the industries employing the 680,602 active professionals in the US with chip manufacturing skills. Panel A focuses on industries directly involved in chip manufacturing, while Panel B highlights the top 10 industries outside of chip manufacturing that also utilize US chip manufacturing talent pool. *Total Emp.* refers to the total number employees with chip manufacturing skills. *Tenure* is the average number of days active employees with chip manufacturing skills have spent in their current position; *RN* represents the average order of a job within an employee's career; *Salary* is the average annual income in USD; and *Seniority* refers to the average seniority level, categorized into seven levels. For more details on the data collection methodology and the definition of chip manufacturing skills, refer to Section B.1.2. For detailed variable definitions, please see Section B.2.

Panel A: Chip Manufacturing Industries

Rank	Industry	NAICS	Total Emp.	Tenure	RN	Salary	Seniority
1	Semiconductor and Related Device Manufacturing	334413	72,512	3,035.24	4.9	113,197.25	3.24
2	Semiconductor Machinery Manufacturing	333242	7,943	3,159.26	4.99	109,462.64	3.34
3	Instrument Mfg. for Electricity & Electrical Signal Testing	334515	6,514	3,719.29	4.73	101,481.78	2.97
4	Printed Circuit Assembly (Electronic Assembly) Manufacturing	334418	1,526	4,054.05	4.32	98,851.70	3.16

Panel B: Other Industries

Rank	Industry	NAICS	Total Emp.	Tenure	RN	Salary	Seniority
1	Software Publishers	511210	35,572	1,811.93	6.42	122,691.03	3.22
2	Colleges, Universities, and Professional Schools	611310	27,661	2,905.84	5.3	78,354.48	2.46
3	Radio/TV Broadcasting & Wireless Communications Equipment Mfg.	334220	14,591	2,227.03	5.55	125,834.12	2.8
4	Internet Publishing and Broadcasting and Web Search Portals	519130	13,512	1,270.00	6.67	136,641.06	2.74
5	Search & Navigation System Instrument Mfg.	334511	12,868	2,978.82	5.28	96,177.27	2.72
6	Other Computer Related Services	541519	10,877	2,421.91	5.89	109,739.59	3.34
7	Engineering Services	541330	10,593	2,565.56	5.4	94,665.02	2.67
8	Surgical and Medical Instrument Manufacturing	339112	9,991	2,822.09	5.69	102,990.94	3.17
9	Other Electronic Component Manufacturing	334419	9,230	3,534.28	4.82	98,744.39	3.03
10	Automobile Manufacturing	336111	8,664	2,253.57	5.92	93,032.16	2.74

Appendix Table B10. **Additional Summary Statistics**

This table presents additional summary statistics for our variables on US chip manufacturing firms and workforce from 2014 to 2022. In Panel A, *Log(Classmates$_{c,d,j,t}$)* is the natural log of the number of unique classmates who finished the same degree d from the same school in country c and year t with someone identified as chip-skilled as of March 2023 and are subsequently employed in job category j. *Log(Avg. Salary$_{c,d,j,t}$)* is the natural log of their average first-job salary, *Avg. Seniority$_{c,d,j,t}$* is the average first-job seniority level, and *Log(Tenure$_{c,d,j,t}$)* is the log of their mean first-job tenure. Section B of the Appendix offers detailed information on the data collection process.

Panel A: Educational Cohorts of Chip Manufacturing Employees

	N	Mean	Median	SD	P5	P95
Log(Classmates$_{c,d,j,t}$)	35,496	1.21	0.69	1.56	0.00	4.44
Log(Avg. Salary$_{c,d,j,t}$)	35,496	6.02	9.42	5.14	0.00	11.29
Avg. Seniority$_{c,d,j,t}$	35,496	1.51	1.50	1.56	0.00	4.33
Log(Tenure$_{c,d,j,t}$)	35,496	3.18	5.02	2.79	0.00	6.19

Appendix Table B11. **Main Findings After Excluding Data Science and Programming Roles**

This table presents our main findings after excluding all data and programming related roles at US chip manufacturing companies, as explained in Section 5.1.1. Our estimates are based on the difference-in-differences approach outlined in Equation (8). Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data collection process. For all variables in Panel B, we set missing values to zero and control for these cases in regressions using an untabulated dummy variable. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.08***	-0.04***	-0.08***
	(-3.51)	(-8.46)	(-4.10)	(-7.52)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,886	68,886	68,886	68,886
R-squared	0.975	0.872	0.861	0.887
Panel B: Analyses of Employment Growth				
	Hiring $\text{Rate}_{i,j,t}$	Separation $\text{Rate}_{i,j,t}$	Net Hiring $\text{Rate}_{i,j,t}$	Turnover $\text{Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.01***	-0.02***	-0.04***
	(-4.55)	(-3.64)	(-2.86)	(-5.08)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,886	68,886	68,886	68,886
R-squared	0.395	0.390	0.343	0.422
Panel C: Analyses of Chip Manufacturing Workforce by Career Progression				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.02	-0.02**	-0.01
	(-4.46)	(-1.64)	(-2.09)	(-0.99)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.983	0.974	0.974	0.973

Appendix Table B12. **Placebo Test: Other Electronic Parts and Equipment Merchant Wholesalers**

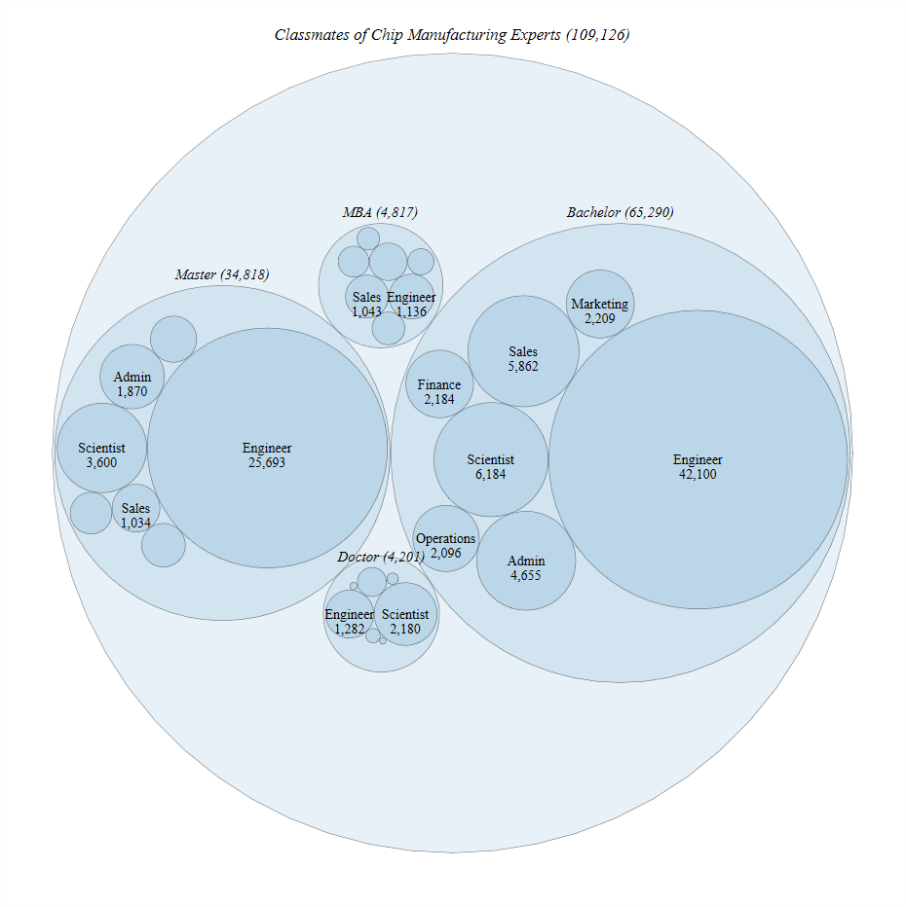
This table presents our findings from our placebo test on how protectionism has influenced science and engineering employment at US chip manufacturing companies, based on firms with NAICS code of 423690 (i.e., merchant wholesale distributors of electronic parts and equipment; except for electrical apparatus and equipment, wiring supplies, and construction materials, electrical and electronic appliances, and television and radio sets). Utilizing the difference-in-differences approach outlined in Equation (8), we analyze the effects on employment metrics. Descriptions of all dependent variables are provided in the caption of Table 1, and Section B of the Appendix offers detailed information on the data collection process. For all variables in Panel B, we set missing values to zero and control for these cases in regressions using an untabulated dummy variable. $Treated_j$ is assigned a value of one for science and engineering job categories, and zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years after 2018 and zero for the preceding years. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by $\star\star\star$, $\star\star$, and $\star$, respectively.

Panel A: Analysis of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	0.00	-0.02	-0.01	-0.02
	(0.14)	(-1.15)	(-0.35)	(-0.87)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	22,311	22,311	22,311	22,311
R-squared	0.967	0.816	0.799	0.842
Panel B: Analyses of Employment Growth				
	$\text{Hiring Rate}_{i,j,t}$	$\text{Separation Rate}_{i,j,t}$	$\text{Net Hiring Rate}_{i,j,t}$	$\text{Turnover Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.01	-0.00	-0.01	-0.01
	(-0.89)	(-0.19)	(-0.81)	(-0.76)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	22,311	22,311	22,311	22,311
R-squared	0.394	0.367	0.344	0.414

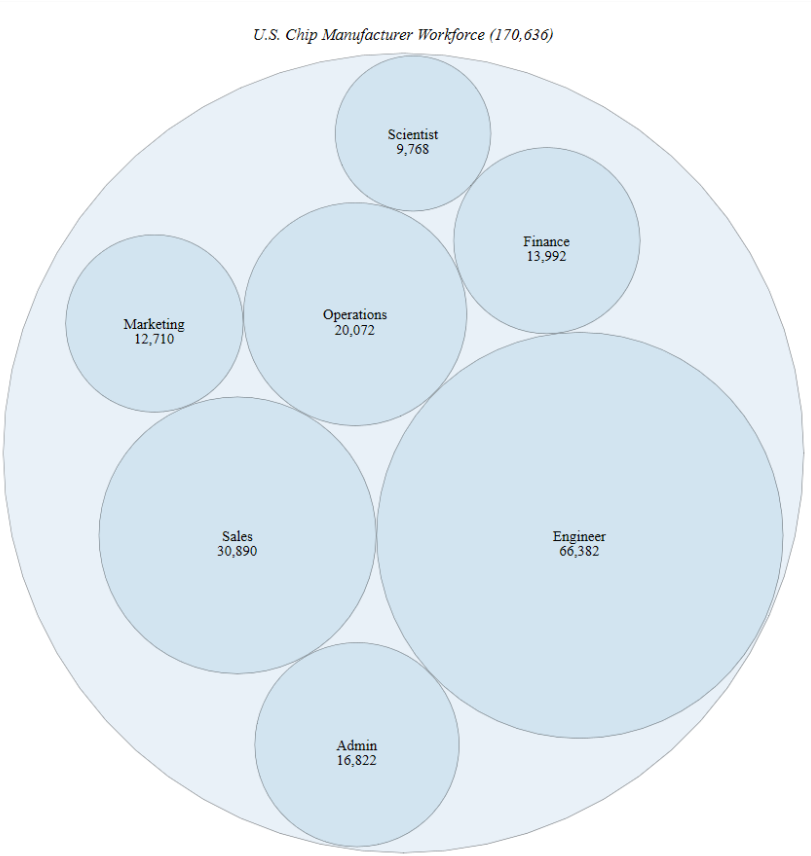
Appendix Figure B1. **U.S. Chip Manufacturing: Workforce Distribution by Job Category**

The figure in Panel A shows the first jobs of students who graduated in the same year, program, and university as individuals with chip manufacturing skills. The analysis is grouped by degree type and initial job category after graduation. Data are as of the end of 2017, excluding categories with fewer than 1,000 classmates. The figure in Panel B displays the aggregate number of employees categorized by job descriptions at US chip manufacturing firms as of the end of 2017. For details on the methodology and variable definitions, please refer to Sections B.1 and B.2.

Panel A: Classmates of Chip Experts and Their Careers

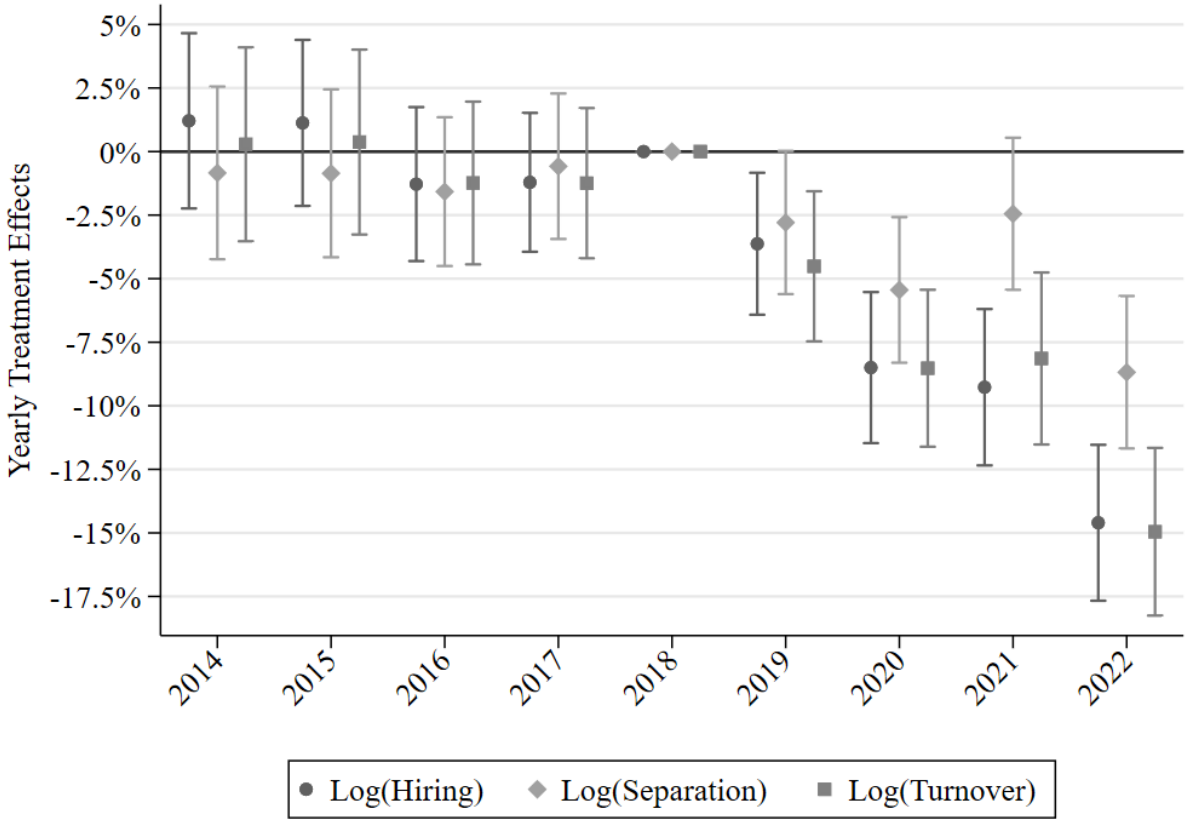


Panel B: Job Categories in US Chip Manufacturing Firms



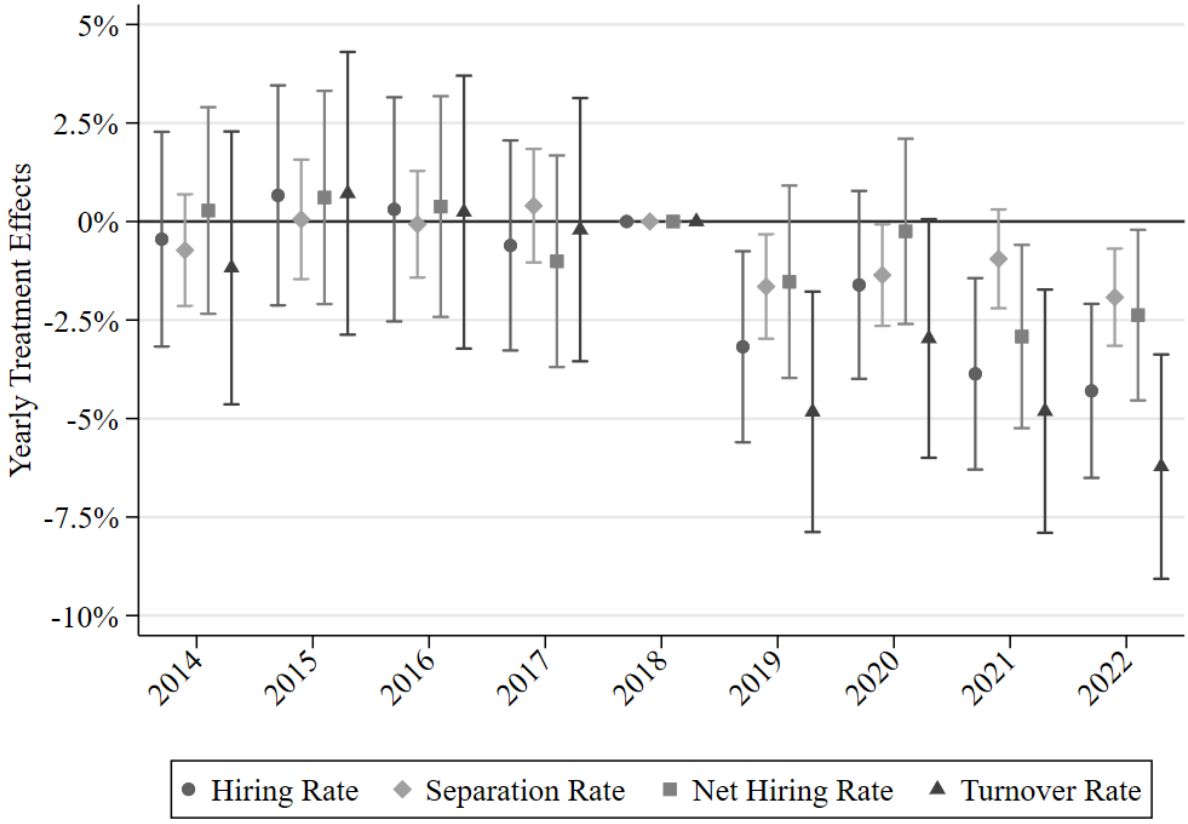
Appendix Figure B2. **Effect Dynamics: Table 2, Panel A**

The figure illustrates the dynamic effects on all other dependent variables listed in Panel A of Table 2 that have not been included in the main text. These effects are calculated using a difference in differences model as in specification (8), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. Section B of the Appendix offers detailed information on the data collection process.



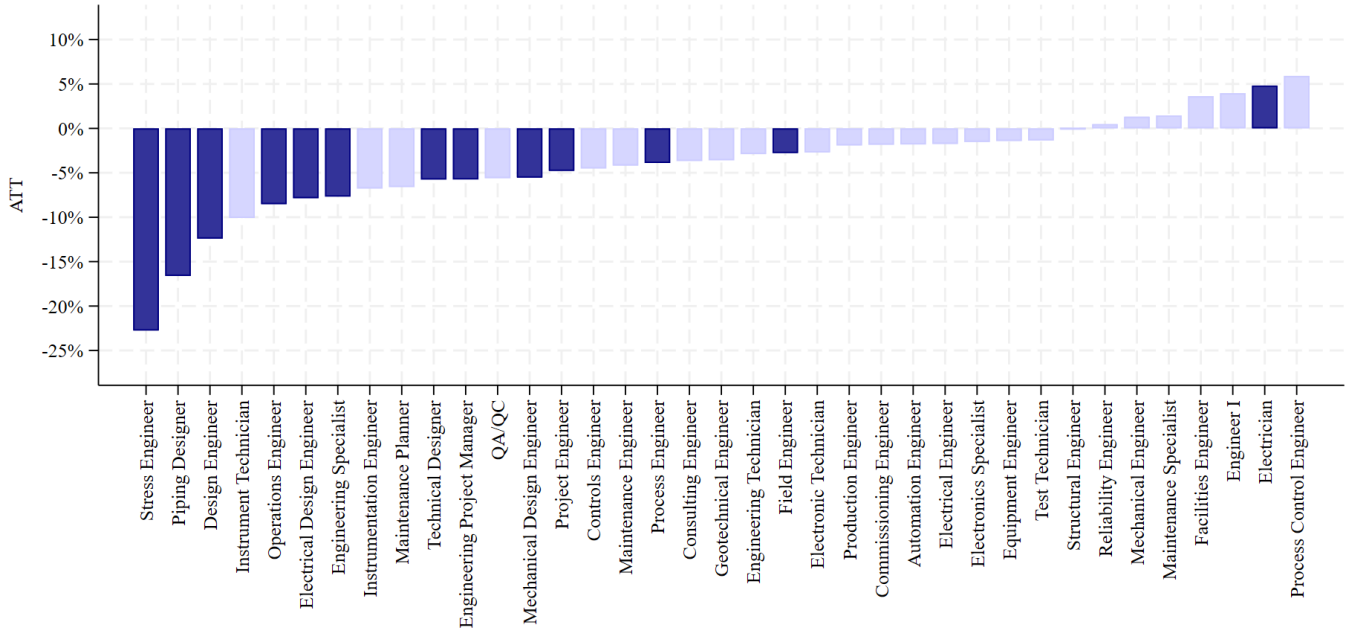
Appendix Figure B3. **Effect Dynamics: Table 2, Panel B**

The figure illustrates the dynamic effects on all other dependent variables listed in Panel B of Table 2 that have not been included in the main text. These effects are calculated using a difference in differences model as in specification (8), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. Section B of the Appendix offers detailed information on the data collection process.



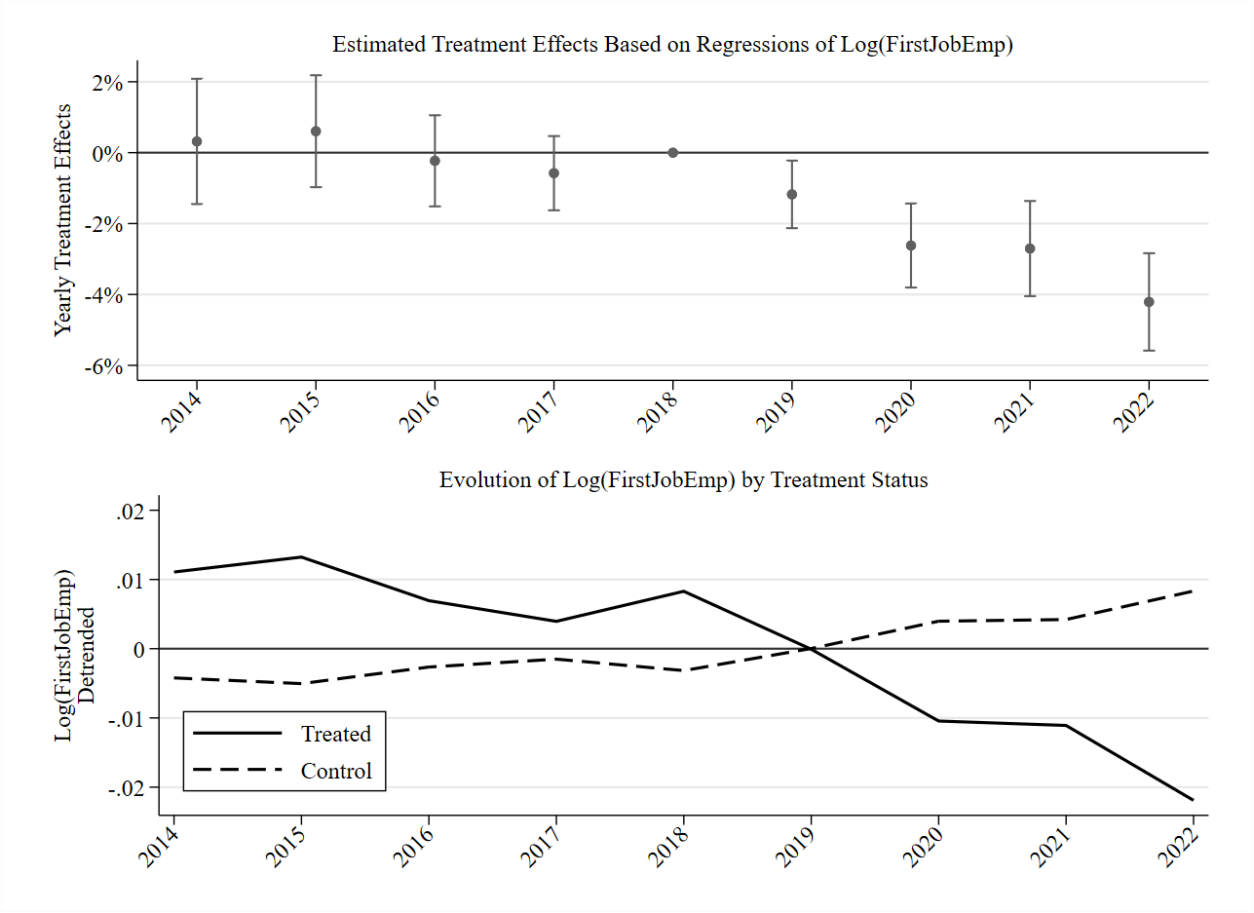
Appendix Figure B4. **Effect Heterogeneity Across Mechanical Engineering Job Categories**

This figure presents additional evidence of effect heterogeneity across Revelio's job categories. We show the effect heterogeneity for roles labeled as *Mechanical Engineer* positions by using Revelio's role_k1000 subcategories. We compare the treated categories to control units, which are non-engineering and non-scientist jobs within the same firm and year, based on Specification (8) and Table 2. Therefore, the estimated ATTs are conditional in the sense that they measure the treatment effects only for firms that employ individuals in each role_k1000 category. The y-axis shows the average treatment effects from our analysis. Bars in darker blue represent statistically significant effects at the 10% level or higher, while light blue bars indicate effects that are not statistically significant. Section B of the Appendix offers detailed information on the data collection process.



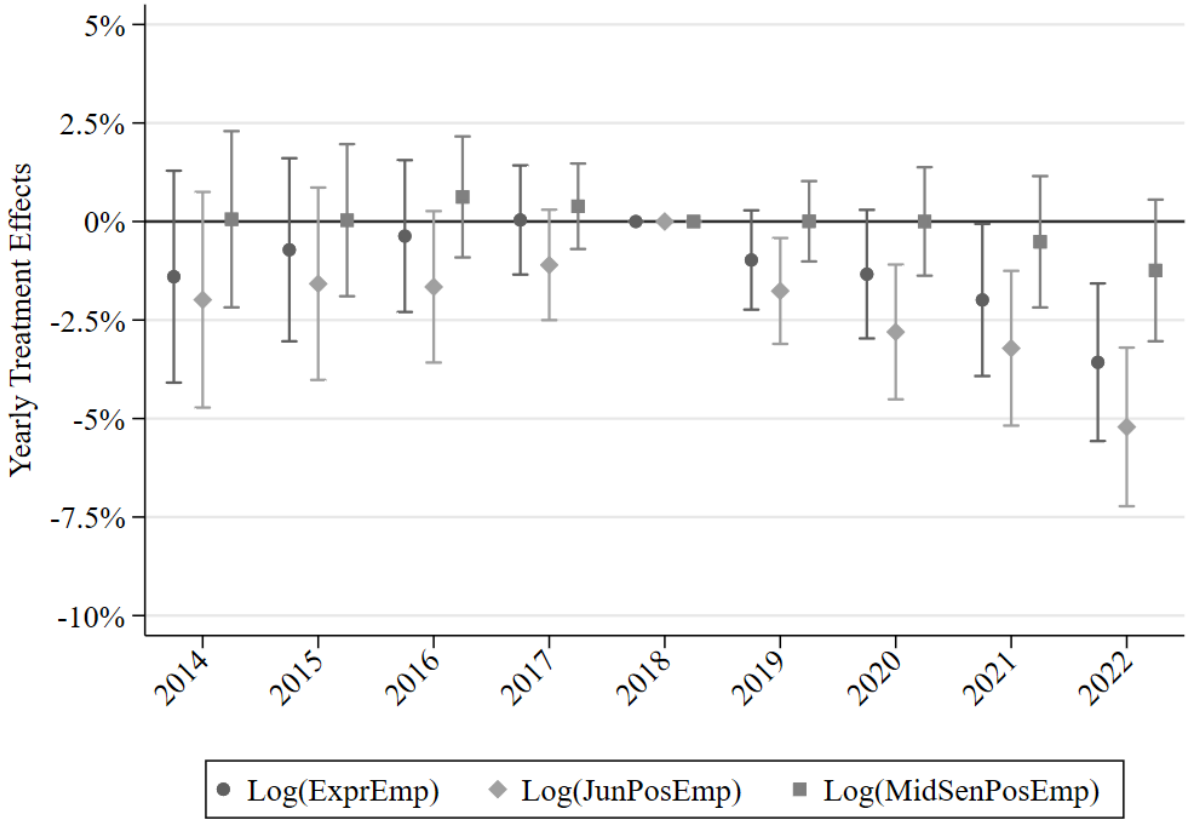
Appendix Figure B5. **Effect Dynamics: First Science and Engineering Jobs at US Chip Manufacturers**

The initial figure illustrates the time-varying effects of US protectionism on the number of first-job employees in engineering and science roles. These effects are calculated using a difference in differences model as in specification (8), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. The second figure displays the evolution of the mean logged number of first-job employees, separately for the treated and control groups. All plotted values are demeaned by year and treatment status. Section B of the Appendix offers detailed information on the data collection process.



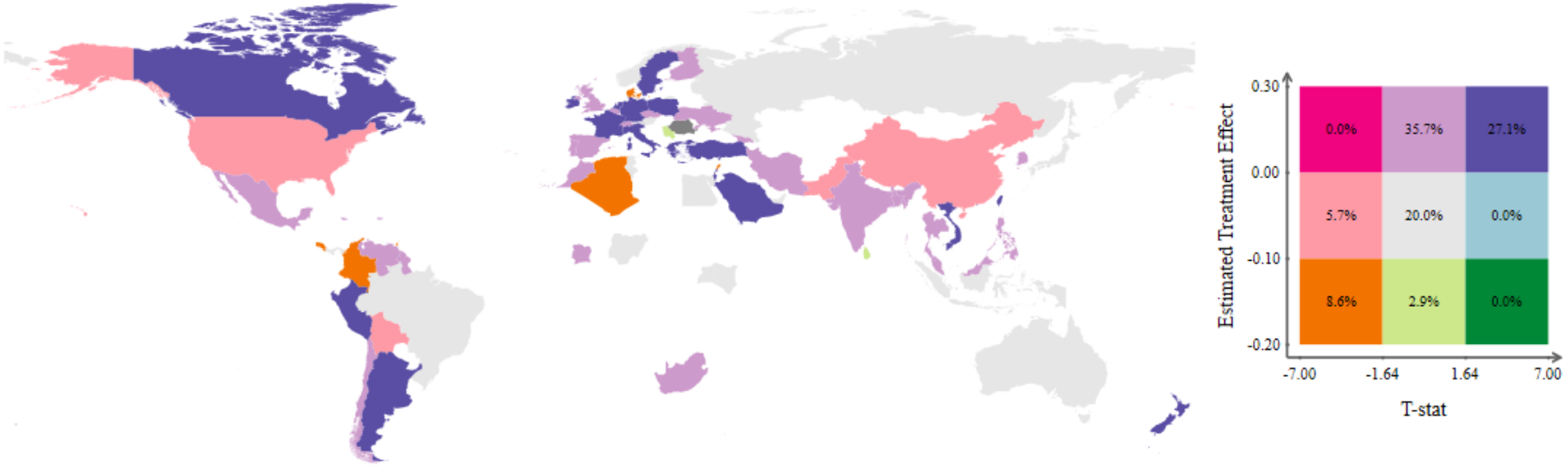
Appendix Figure B6. **Effect Dynamics: Table 2, Panel C**

The figure illustrates the dynamic effects on all other dependent variables listed in Panel C of Table 2 that have not been included previously. These effects are calculated using a difference in differences model as in specification (8), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. Section B of the Appendix offers detailed information on the data collection process.



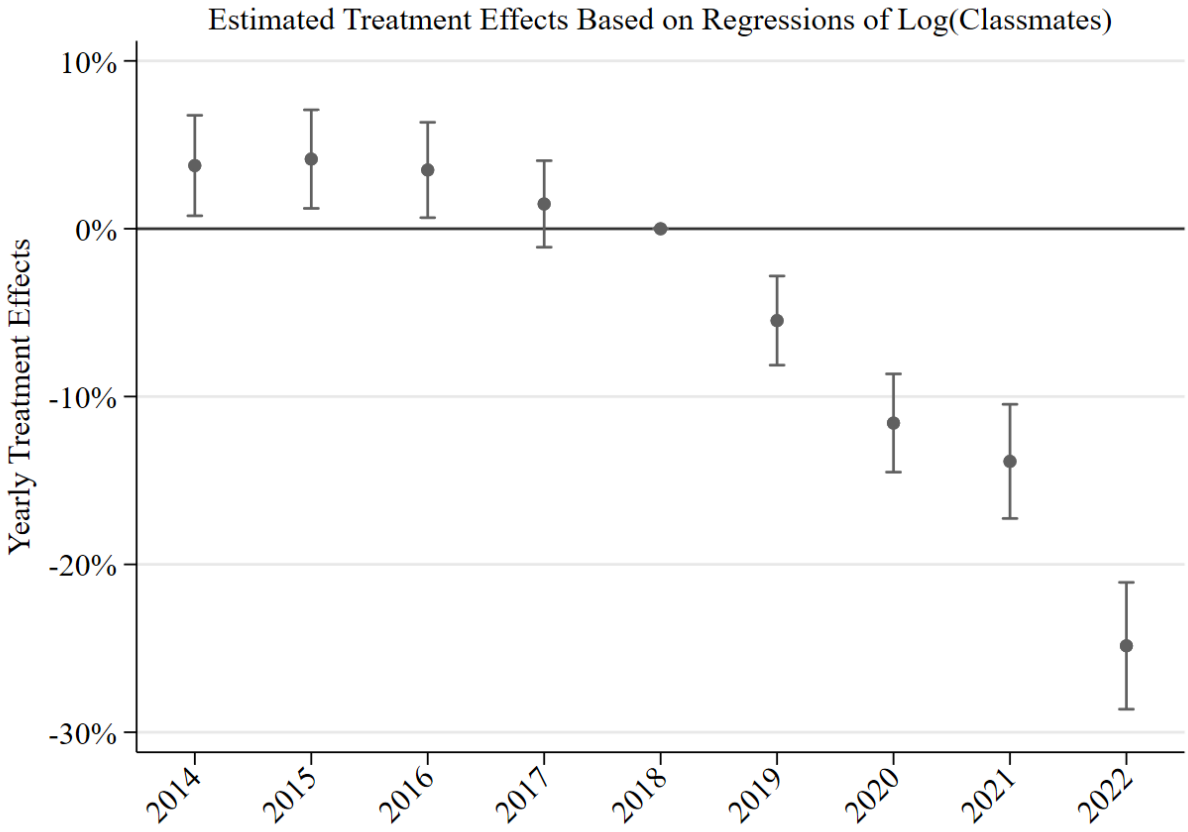
Appendix Figure B7. **Effect Heterogeneity: Global Workforce Trends in US Chip Manufacturers**

This figure shows the outcomes of using Equation (9), incorporating fixed effects only for firm by country by job category and firm by year, with each country analyzed separately. The results are shown visualized on a bivariate world map, where the estimated effects are shown on the y-axis and the t-stats of these estimated effects on the x-axis, with different color labels distinguishing the results. The matrix within the figure indicates the percentage of countries falling into each category, written in black. Countries with no data are shown in white. Section B of the Appendix offers detailed information on the data collection process.



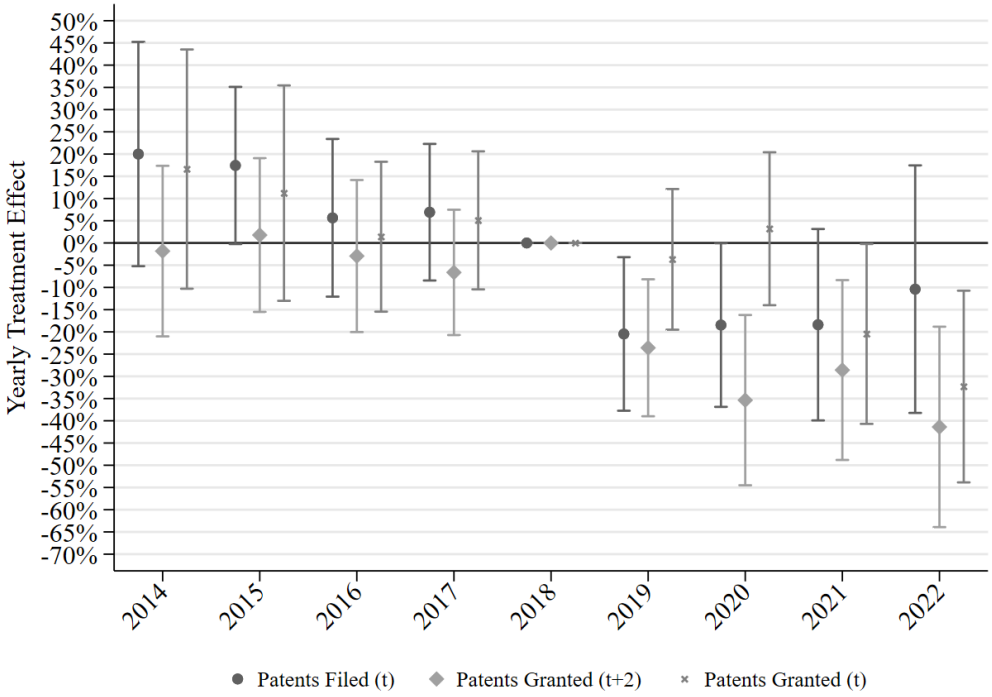
Appendix Figure B8. **Effect Dynamics: Classmates' Shift Away from Chip Manufacturing**

This figure highlights time-varying effects of protectionism on the number of classmates of individuals skilled in chip manufacturing, landing science and engineering jobs. These estimates are based on a difference in differences approach according to specification (11), which accounts for fixed effects across country × job category × degree, country × year, and degree × year. Each point estimate is provided alongside a 95% confidence interval. Section B of the Appendix offers detailed information on the data collection process.



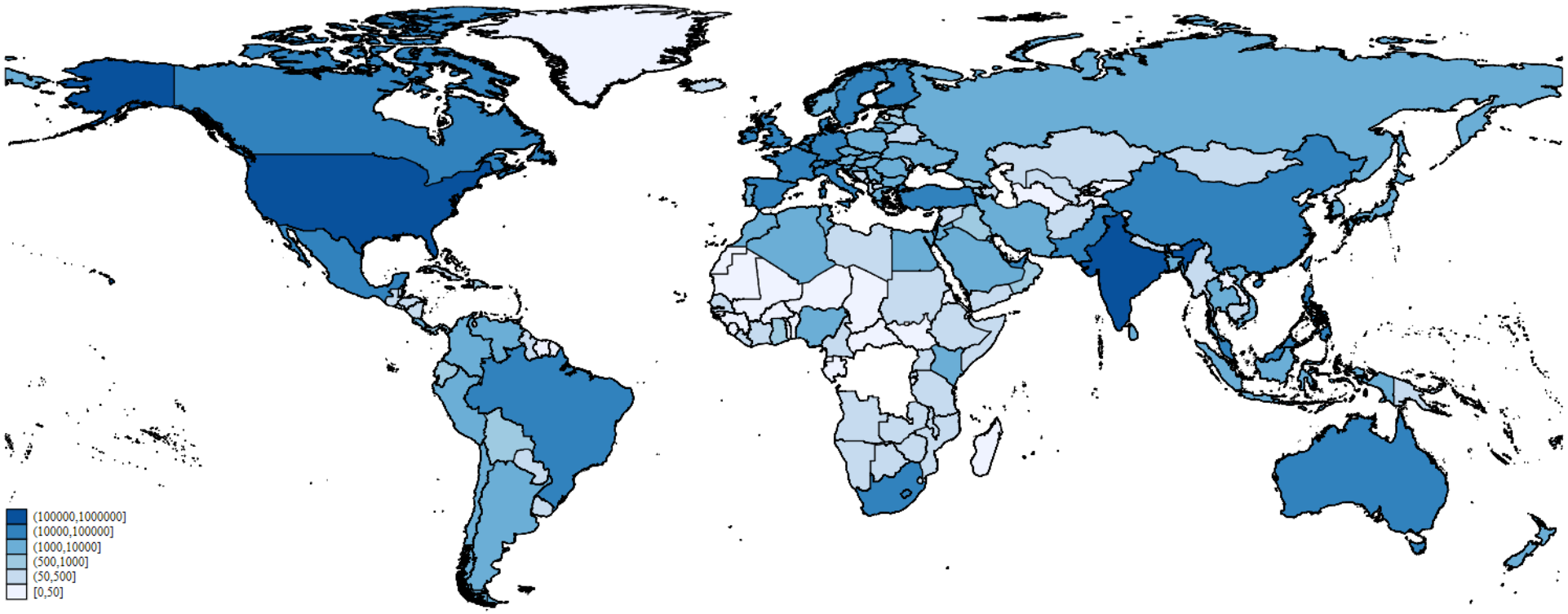
Appendix Figure B9. **Effect Dynamics: Protectionism and Patenting Outcomes Based on Poisson Pseudo-Maximum-Likelihood (PPML) Regressions**

This figure presents our findings on effect dynamics corresponding to Table B5. Our estimates are derived from a Poisson pseudo-likelihood regression with multiple levels of fixed effects (Correia et al., 2020). The effects are based on an interaction between a US firm indicator and year dummies. All regressions include firm fixed effects and industry-by-year fixed effects, with observations weighted by the inverse of firm age in 2014. The plots display 95% confidence intervals. Section B of the Appendix offers detailed information on the data collection process.



Appendix Figure B10. **Active Employees with Chip Manufacturing Skills**

This figure illustrates the global distribution of employees with chip manufacturing skills who are actively employed as of March 2023. Methodological details and definitions regarding chip manufacturing skills are available in Section B.



Appendix Figure B11. **US Share of Chip Manufacturing Skills**

This figure presents the list of skills utilized to identify individuals with chip manufacturing expertise, alongside the percentage representation of each skill among employees in the US. Methodological details and definitions regarding chip manufacturing skills are available in Section B.

